DAC1628D1G25

Dual 16-bit DAC: JESD204B interface: up to 1.25 Gsps; x2, x4 and x8 interpolating

Rev. 1.1 — 10 October 2011 **Objective data sheet**

1. General description

The DAC1628D1G25 is a high-speed high-performance 16-bit dual channel digital-to-analog converter (DAC). The device provides a sample rate up to 1.25 Gsps with selectable 2×, 4× and 8× interpolation filters optimized for multi-carrier and broadband wireless transmitters.

The DAC1628D1G25 integrates a CVGxpress high-speed serial input data interface running up to 6.25 Gbps allowing dual channel input sampling at up to 625 Msps over four differential lanes. CGVXpress is fully compliant with the JEDEC JESD204B standard. It offers numerous advantages over traditional parallel digital interfaces:

- Easier Printed-Circuit Board (PCB) layout
- Lower radiated noise
- Lower pin count
- Self-synchronous link
- Skew compensation
- Deterministic latency
- Multiple Device Synchronization (MDS)
- Harmonic clocking support
- Assured FPGA interoperability

An optional on-chip digital modulation converts the complex I/Q pattern from baseband to IF. The mixer frequency is set by writing to the Serial Peripheral Interface (SPI) control registers associated with the on-chip 40-bit Numerically Controlled Oscillator (NCO). This accurately places the IF carrier in the frequency domain. The 16-bit phase adjustment feature, the 12-bit digital gain and the 16-bit digital offset enable full control of the analog output signals.

The DAC1628D1G25 is fully compliant with device subclass 1 of the JEDEC JESD204B standard, guaranteeing deterministic and repeatable interface latency using the differential SYSREF signal. The device also supports harmonic clocking to reduce system-level clock synthesis and distribution challenges.

Multiple Device Synchronization (MDS, a unique CGVxpress feature) enables up to 16 DAC channels to be sample synchronous and phase coherent to within one DAC clock period. MDS is ideal for LTE and LTE-A MIMO transceiver applications.

The DAC1628D1G25 includes a ×2, ×4 or ×8 clock multiplier which provides the appropriate internal clocks and an internal regulation to adjust the full-scale output current. The internal PLL can be bypassed to achieve the best possible noise performance at the analog outputs. The internal regulator adjusts the full-scale output current between 8.1 mA and 34 mA.

The device is available in a HVQFN56 package (8 mm × 8 mm). It is supported by customer demo boards that are supplied with or without FPGA logic devices.

2. Features and benefits

- Dual channel 16-bit resolution
- 1.25 Gsps maximum output update rate
- JEDEC JESD204B device subclass I compliant: SYSREF based deterministic and repeatable interface latency
- Multiple Device Synchronization (MDS, a unique CGVxpress feature) enables up to 16 DAC channels to be sample synchronous and phase coherent to within one DAC clock period
- 1, 2 or 4 configurable JESD204B serial input lanes running up to 6.25 Gbps with embedded termination and programmable equalization
- 625 Msps maximum baseband input data rate
- SPI interface (3-wire or 4-wire mode) for control setting and status monitoring
- Differential scalable output current from 8.1 mA to 34 mA
- Embedded NCO with 40-bit programmable frequency and 16-bit phase adjustment
- Embedded complex (IQ) digital modulator
- 1.8 V and 3.3 V power supplies
- $SFDR_{RBW}$ = 85 dBc typical (f_s = 1.22 Gsps; interpolation ×4; bandwidth = 250 MHz; f_{out} = 150 MHz)
- NSD = −164 dBm/Hz typical (f_o = 20 MHz)
- IMD3 = 85 dBc typical (f_s = 1.22 Gsps; interpolation ×4; f_{o1} = 152 MHz; f_{o2} = 155.1 MHz)
- One carrier ACLR = 77 dB typical (f_s = 1.22 Gsps; f_{NCO} = 210 MHz)
- RF enable/disable pin and RF automatic mute
- Very low noise bypassable integrated Phase-Locked Loop (PLL); no external capacitors
- External analog offset control (10-bit auxiliary DACs)
- power-down mode and sleep mode controls
- On-chip 1.25 V reference
- Industrial temperature range −40 °C to +85 °C
- HVQFN56 package (8 mm × 8 mm)

3. Applications

- Wireless infrastructure radio base station transceivers, including: LTE-A, LTE, MC_GSM, W-CDMA, TD-SCDMA
- LMDS/MMDS, point-to-point microwave backhaul
- Direct Digital Synthesis (DDS) instruments
- High-definition video broadcast production equipment
- Automated Test Equipment (ATE)

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
DAC1628D1G25HN	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; 8 × 8 × 0.85 mm	SOT684-8

5. Block diagram

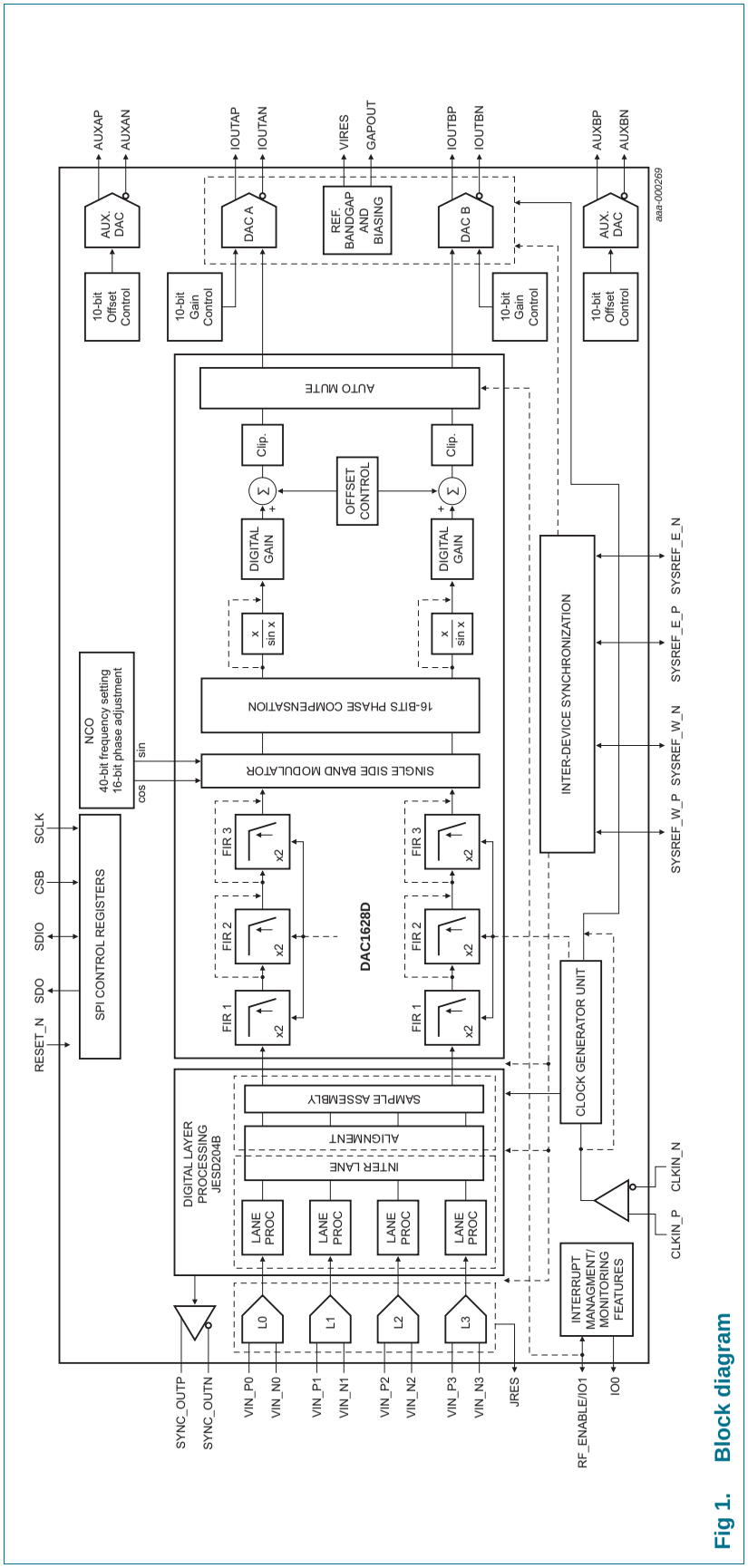


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

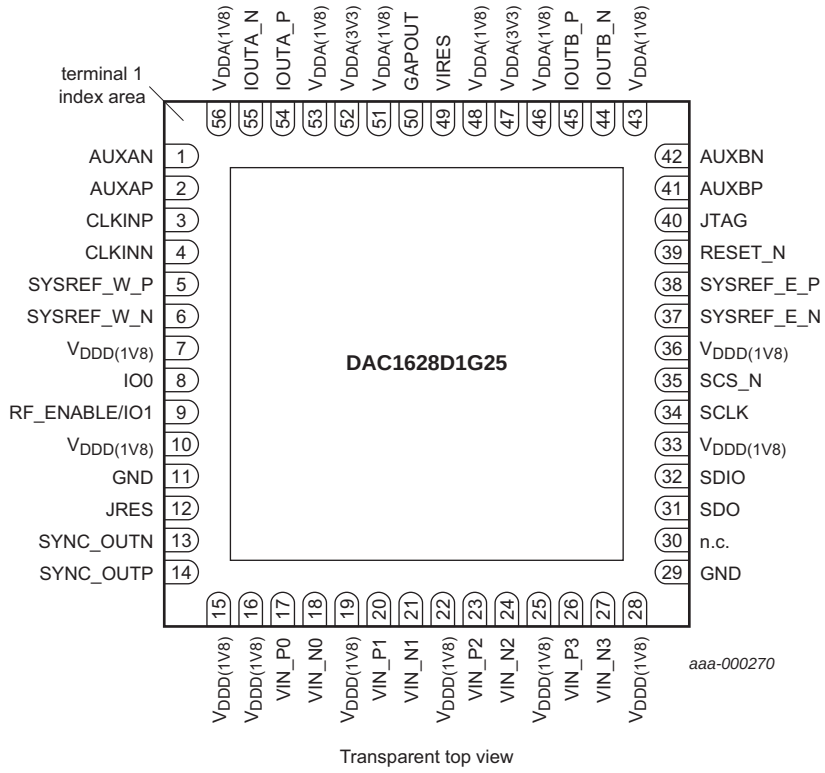


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
AUXAP	1	O	auxiliary DAC A output current
AUXAN	2	O	complementary auxiliary DAC A output current
CLKINP	3	I	DAC clock positive input
CLKINN	4	I	DAC clock negative input
SYSREF_W_P	5	I/O	multiple devices synchronization positive signal, west side
SYSREF_W_N	6	I/O	multiple devices synchronization negative signal, west side
VDDD(1V8)	7	P	1.8 V digital power supply
IO0	8	O	IO port bit 0
RF_ENABLE/IO1	9	I/O	IO port bit 1 or RF enable pin (see Section automute)
$V_{DDD(1V8)}$	10	P	1.8 V digital power supply
GND	11	G	connect to ground
JRES	12	I/O	Calibration resistor (12.5 kΩ) for serial lanes termination

Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Description
SYNC_OUTN	13	O	synchronization request to transmitter, complementary output
SYNC_OUTP	14	O	synchronization request to transmitter
$V_{DDD(1V8)}$	15	P	1.8 V digital power supply for JESD204B SYNCB/reference interface
$V_{DDD(1V8)}$	16	P	1.8 V digital power supply for JESD204B Lane 0
VIN_P0	17	[2]	serial interface lane 0 positive input
VIN_N0	18	[2]	serial interface lane 0 negative input
$V_{DDD(1V8)}$	19	P	1.8 V digital power supply for JESD204B Lane 0 and Lane 1
VIN_P1	20	[2]	lane 1 serial interface positive input
VIN_N1	21	[2]	serial interface lane 1 negative input
$V_{DDD(1V8)}$	22	P	1.8 V digital power supply for JESD204B Lane 1 and Lane 2
VIN_P2	23	[2]	serial interface lane 2 positive input
VIN_N2	24	[2]	serial interface lane 2 negative input
$V_{DDD(1V8)}$	25	P	1.8 V digital power supply for JESD204B Lane 2 and Lane 3
VIN_P3	26	[2]	serial interface lane 3 positive input
VIN_N3	27	[2]	serial interface lane 3 negative input
$V_{DDD(1V8)}$	28	P	1.8 V digital power supply for JESD204B Lane 3
GND	29	G	connect to ground
n.c.	30	-	not connected
SDO	31	I	SPI data output
SDIO	32	I/O	SPI data input/output
$V_{DDD(1V8)}$	33	P	1.8 V digital power supply
SCLK	34	I	SPI clock
SCS_N	35	I	SPI chip select (active LOW)
$V_{DDD(1V8)}$	36	P	1.8 V digital power supply
SYSREF_E_N	37	I/O	multiple devices synchronization negative signal, east side
SYSREF_E_P	38	I/O	multiple devices synchronization positive signal, east side
RESET_N	39	I	general reset (active LOW)
JTAG	40	G	JTAG connection (connect to ground)
AUXBP	41	O	auxiliary DAC B output current
AUXBN	42	O	complementary auxiliary DAC B output current
$V_{DDA(1V8)}$	43	P	1.8 V analog power supply
IOUTBN	44	O	DAC B output current
IOUTBP	45	O	complementary DAC B output current
$V_{DDA(1V8)}$	46	P	1.8 V analog power supply
$V_{DDA(3V3)}$	47	P	3.3 V analog power supply
$V_{DDA(1V8)}$	48	P	1.8 V PLL analog power supply
VIRES	49	I/O	DAC biasing resistor
GAPOUT	50	I/O	band gap input/output voltage
$V_{DDA(1V8)}$	51	P	1.8 V PLL analog power supply

Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Description
$V_{DDA(3V3)}$	52	P	3.3 V analog power supply
$V_{DDA(1V8)}$	53	P	1.8 V analog power supply
IOUTAP	54	O	complementary DAC A output current
IOUTAN	55	O	DAC A output current
$V_{DDA(1V8)}$	56	P	1.8 V analog power supply

[1] P: power supply; G: ground; I: input; O: output.

[2] JESD204B input lanes can be swapped between P and N using dedicated registers. The order of lanes can be updated logically.

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		–0.5	+4.6	V
$V_{DDD(1V8)}$	digital supply voltage (1.8 V)		–0.5	+2.5	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V)		–0.5	+2.5	V
V_I	input voltage	input pins referenced to GND	–0.5	<tbd>	V
V_O	output voltage	pins IOUTAP, IOUTAN, IOUTBP, IOUTBN, AUXAP, AUXAN, AUXBP and AUXBN; referenced to GND	–0.5	+4.6	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		–40	+125	°C

8. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
JEDEC 4L board					
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	19	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1]	<tbd>	K/W

Table 4. Thermal characteristics *…continued*

Symbol	Parameter	Conditions		Typ	Unit
Application board					
$R_{th(j-a)}$	thermal resistance from junction to ambient	6 layers	[2]	15.9	K/W
		8 layers	[2]	15.6	K/W
		12 layers	[2]	14.0	K/W

[1] In compliance with JEDEC test board; in free air with 64 thermal vias, class 5.

[2] In free air with 64 thermal vias, class 5.

9. Characteristics

Table 5. Characteristics

V_{DDA1V8} = 1.8 V; V_{DDD1V8} = 1.8 V; V_{DDA3V3} = 3.3 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate used; external PLL; no auxiliary DAC; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		C	3.15	3.3	3.45	V
$V_{DDD(1V8)}$	digital supply voltage (1.8 V)		C	1.7	1.8	1.9	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V		C	1.7	1.8	1.9	V
$I_{DDA(3V3)}$	analog supply current (3.3 V)	Auxiliary DAC on	C	<tbd>	63	<tbd>	mA
$I_{DDD(1V8)}$	digital supply current (1.8 V)	f_s = 1228.8 Msps; ×2 interpolation; NCO on; MDS off; 4 JESD204B lanes	C	<tbd>	822	<tbd>	mA
		fs = 983.04 Msps; ×4 interpolation; no NCO; MDS on; 4 JESD204B lanes	C	<tbd>	<tbd>	<tbd>	mA
		f_s = 620 Msps; ×2 interpolation; NCO on; no MDS; 2 JESD204B lanes	C	<tbd>	<tbd>	<tbd>	mA
$I_{DDA(1V8)}$	analog supply current (1.8 V)	f_s = 1228.8 Msps; 1 V (p-p)	C	<tbd>	210	<tbd>	mA
		f_s = 983.04 Msps; 1 V (p-p)	C	<tbd>	210	<tbd>	mA
		f_s = 620 Msps; 1 V (p-p);	C	<tbd>	210	<tbd>	mA

Table 5. Characteristics *...continued*

V_{DDA1V8} = 1.8 V; V_{DDD1V8} = 1.8 V; V_{DDA3V3} = 3.3 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate used; external PLL; no auxiliary DAC; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
Power dissipation							
P_{tot}	total power dissipation	f_s = 1228.8 Msps; ×2 interpolation; NCO on; MDS off	C	-	2272	-	mW
		four JESD204B lanes					
		f_s = 1228.8 Msps; ×4 interpolation; NCO off; MDS on	C	-	<tbd>	-	mW
		f_s = 983.04 Msps; ×4 interpolation; NCO off; MDS on	C	-	<tbd>	-	mW
		f_s = 983.04 Msps; ×4 interpolation; NCO off; MDS on	C	-	<tbd>	-	mW
		f_s = 737.28 Msps; ×4 interpolation; NCO on; MDS on	C	-	<tbd>	-	mW
		f_s = 620 Msps; ×2 interpolation; NCO on; no MDS;	C	-	<tbd>	-	mW
		full power-down	C	-	1.2	-	mW
		DAC A and DAC B Sleep mode; ×8 interpolation; NCO on	C	-	<tbd>	-	W
Clock inputs (pins CLKINP, CLKINN)							
V_i	input voltage	$\|V_{gpd}\|$ < 50 mV	C	[2] 825	-	1575	mV
V_{idth}	input differential threshold voltage	$\|V_{gpd}\|$ < 50 mV	C	[2] −100	-	+100	mV
R_i	input resistance		D	-	<tbd>	-	MΩ
C_i	input capacitance		D	-	<tbd>	-	pF
Digital inputs/outputs (SYSREF_W_P/SYSREF_W_N, SYSREF_E_P/SYSREF_E_N)							
V_i	input voltage	$\|V_{gpd}\|$ < 50 mV	C	[2] 825	-	1575	mV
V_{idth}	input differential threshold voltage	$\|V_{gpd}\|$ < 50 mV	C	[2] −100	-	+100	mV
R_i	input resistance		D	-	100	-	Ω
C_i	input capacitance		D	-	<tbd>	-	pF

Table 5. Characteristics *...continued*

V_{DDA1V8} = 1.8 V; V_{DDD1V8} = 1.8 V; V_{DDA3V3} = 3.3 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate used; external PLL; no auxiliary DAC; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
Digital inputs (pins SDO, SDIO, SCLK, SCS_N, RESET_N)							
V_{IL}	LOW-level input voltage		C	GND	-	$0.3V_{DDD(1V8)}$	V
V_{IH}	HIGH-level input voltage		C	$0.7V_{DDD(1V8)}$	-	$V_{DDD(1V8)}$	V
I_{IL}	LOW-level input current	V_{IL} = <tbd> V	I	-	<tbd>	-	µA
I_{IH}	HIGH-level input current	V_{IH} = <tbd> V	I	-	<tbd>	-	µA
Digital outputs (pins SDO, SDIO)							
V_{OL}	LOW-level output voltage		C	<tbd>	-	<tbd>	V
V_{OH}	HIGH-level output voltage		C	<tbd>	-	<tbd>	V
Analog outputs (pins IOUTAP, IOUTAN, IOUTBP, IOUTBN)							
$I_{O(fs)}$	full-scale output current		D	8.1	-	34	mA
			D	-	20	-	mA
V_O	output voltage		D	<tbd>	-	$V_{DDA(3V3)}$	V
$V_{O(cm)}$	common-mode output voltage		D	-	2.8	-	V
R_o	output resistance		D	0	250	-	kΩ
C_o	output capacitance		D	-	3	-	pF
$N_{DAC(mono)}$	DAC monotonicity	guaranteed	D	-	<tbd>	-	bits
ΔE_O	offset error variation		D	-	<tbd>	-	ppm/°C
ΔE_G	gain error variation		D	-	<tbd>	-	ppm/°C
Reference voltage output (pin GAPOUT)							
$V_{O(ref)}$	reference output voltage	T_{amb} = 25 °C	I	<tbd>	1.25	<tbd>	V
$I_{O(ref)}$	reference output current	external voltage = 1.25 V	D	-	40	-	µA
$\Delta V_{O(ref)}$	reference output voltage variation		D	-	<tbd>	-	ppm/°C
Analog auxiliary outputs (pins AUXAP, AUXAN, AUXBP and AUXBN)							
$I_{O(fs)}$	full-scale output current	auxiliary DAC A; differential inputs	I	-	3.1	-	mA
		auxiliary DAC B; differential inputs	I	-	3.1	-	mA

Table 5. Characteristics *...continued*

V_{DDA1V8} = 1.8 V; V_{DDD1V8} = 1.8 V; V_{DDA3V3} = 3.3 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate used; external PLL; no auxiliary DAC; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
$V_{O(aux)}$	auxiliary output voltage		C	0	-	2	V
$N_{DAC(aux)mono}$	auxiliary DAC monotonicity	guaranteed	D	-	10	-	bits
DAC Output timing							
f_s	sampling rate		C	-	-	1250	Msps
t_s	settling time	to = ±0.5LSB	D	-	20	-	ns
NCO frequency range; f_s = 1000 Msps							
f_{NCO}	NCO frequency	two's complement coding					
		register value = 8000000000h	D	-	−500	-	MHz
		register value = FFFFFFFFFFh	D	-	−0.9095	-	mHz
		register value = 0000000000h	D	-	0	-	Hz
		register value = 0000000001h	D	-	+0.9095	-	mHz
		register value = 7FFFFFFFFFh	D	-	+499.999 09	-	MHz
f_{step}	step frequency		D	-	0.9095	-	mHz
Low power NCO frequency range; f_s = 1000 Msps (see Section 10.7.2)							
f_{NCO}	NCO frequency	two's complement coding					
		register value = 8000000000h	D	-	−500	-	MHz
		register value = F800000000h	D	-	-31.25	-	MHz
		register value = 0000000000h	D	-	0	-	Hz
		register value = 0800000000h	D	-	+31.25	-	MHz
		register value = 7800000000h	D	-	+468.75	-	MHz
f_{step}	step frequency		D	-	31.25	-	MHz

Table 5. Characteristics *...continued*

V_{DDA1V8} = 1.8 V; V_{DDD1V8} = 1.8 V; V_{DDA3V3} = 3.3 V; Typical values measured at T_{amb} = +25 °C; R_L = 50 Ω; $I_{O(fs)}$ = 20 mA; maximum sample rate used; external PLL; no auxiliary DAC; no inverse (sinus x) / x; no output correction; output level = 1 V (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
Dynamic performance							
SFDR	spurious-free dynamic range	f_{data} = 307.2 MHz; f_s = 1228.8 Msps; B = f_s / 2;					
		f_o = 20 MHz at −1 dBFS	I	-	83	-	dBc
		f_{data} = 245.76 MHz; f_s = 983.04 Msps; B = f_s / 2					
		f_o = 20 MHz at −1 dBFS	I	-	85	-	dBc
$SFDR_{RBW}$	restricted bandwidth spurious-free dynamic range	f_o = 150 MHz; f_s = 983.04 Msps					
		B = 100 MHz	I	-	85	-	dBc
		B = 180 MHz	I	-	85	-	dBc
IMD3	third-order intermodulation distortion	f_{o1} = 152.1 MHz; f_{o2} = 155.1 MHz; −7 dBFS; f_s = 1228.8 Msps; ×4 interpolation	I	-	85	-	dBc
		f_{o1} = 20 MHz; f_{o2} = 21 MHz; −7 dBFS; f_s = 1228.8 Msps; ×4 interpolation	I	-	93	-	dBc
ACPR	adjacent channel power ratio	f_s = 1228.8 Msps; ×4 interpolation; f_o = 210 MHz					
		2 carriers; B = 10 MHz	D	-	73	-	dBc
		4 carriers; B = 20 MHz	D	-	72	-	dBc
NSD	noise spectral density	f_s = 983.04 Msps; ×4 interpolation; f_o = 20 MHz at −1 dBFS	D	-	−164	-	dBm/Hz
		f_s = 983.04 Msps; ×4 interpolation; f_o = 147 MHz at −1 dBFS	D	-	−161	-	dBm/Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

[2] $|V_{gpd}|$ represents the ground potential difference voltage. This is the voltage that results from current flowing through the finite resistance and the inductance between the receiver and the driver circuit ground voltages.

10. Application information

10.1 General description

The DAC1628D1G25 is a dual 16-bit DAC operating up to 1.25 Gsps. A maximum input data rate up to 625 Msps ensures more flexibility for wideband and multicarrier systems. The incorporated quadrature modulator and 40-bit Numerically Controlled Oscillator (NCO) simplifies the frequency selection of the system. This is also possible because of the ×2, ×4 or ×8 interpolation filters which remove undesired images.

The DAC1628D1G25 supports the following JESD204B key features:

- 10-bit/8-bit decoding
- Code group synchronization
- Inter-Lane Alignment (ILA)
- $1 + x^{14} + x^{15}$ scrambling polynomial
- Character replacement
- TX/RX synchronization management via synchronization signals
- Multiple Converter Device Alignment-Multiple Lanes (MCDA-ML) device
- number L of serial lanes: 1, 2, 4
- number M of data converters: 1 or 2
- number F of octets per frame: 1, 2, 4
- number S of samples per frame: 1, 2

The DAC1628D1G25 can be interfaced with any logic device that features high-speed SERializer/DESerializer (SERDES) functionality. This macro is now widely available in Field-Programmable Gate Array (FPGA) of different vendors. Standalone SERDES ICs can also be used.

NXP includes polarity swapping for each of the lanes and additionally offers lane swapping to enhance the intrinsic board layout simplification of the JESD204B standard. Each physical lane can be configured logically as lane 0, lane 1, lane 2 or lane 3.

This device is MCDA-ML compliant, offering inter-lane alignment between several devices. An NXP proprietary mechanism in combination with the JESD204B subclass I clause enables maintenance of sample alignment between devices up to output level. Output samples are automatically aligned to the SYSREF signal generated by a dedicated IC or by the FPGA itself. A system with several DAC1628D1G25s can produce data with a guaranteed alignment of less than 1 DAC output clock period. The DAC1628D1G25 incorporates two differential SYSREF ports (located at the East and West side of the IC). These can be programmed to act as an input or an output regarding the mode expected for the system (Normal mode, Daisy chain). The device also enables independent link reinitialization.

Each DAC generates two complementary current outputs on pins IOUTAP/IOUTAN and IOUTBP/IOUTBN, providing a nominal full-scale output current of 20 mA. An internal reference is available for the reference current which is externally adjustable using pin VIRES.

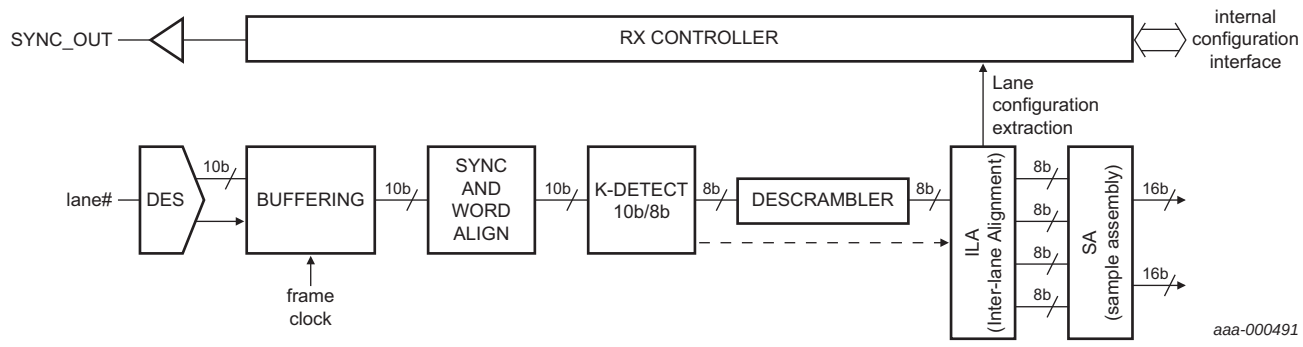
Configure the DAC1628D1G25 before operating. It features an SPI slave interface to access the internal registers. Some of these registers also provide information about the JESD204B interface status. Optionally, an interrupt capability can be programmed using those registers to ensure ease of use of the device.

Because of the JESD204B standardization, the DAC1628D1G25 does not require any adjustment from the Transmit Logic Device (TLD) to capture the input data streams. Some autolock features can be monitored using the SPI registers.

A new NXP automute feature enables switching off of the RF output signal as a result of various internal events occurring.

The DAC1628D1G25 requires supplies of both 3.3 V and 1.8 V. The 1.8 V supply has separate digital and analog power supply pins.

10.2 JESD204B receiver



The descrambler can be enabled or disabled.

Fig 3. JESD204B receiver

The JESD204B defines the following parameters:

- L is the number of lanes per link
- M is the number of converters per device
- F is the number of octets per frame clock period

The variable delay (latency uncertainty) is the result of uncertainties and variation in design implementations along the path between the transmit logic device and the DAC1628D1G25. The Inter-Lane Alignment (ILA) module present in Digital Layer Processing (DLP) realigns the input streams to the last data received.

Table 6. Digital layer processing latency

Symbol	Parameter	Conditions	Test[1]	Min	Typ	Max	Unit
t_d	delay time	digital layer processing delay	D	<tbd>	-	<tbd>	cycle[2]

[1] D = guaranteed by design.

[2] Frame clock cycle.

10.2.1 Lane input

Each lane is Current Mode Logic (CML) compliant. It is terminated to a common voltage with an integrated 50 Ω resistor.

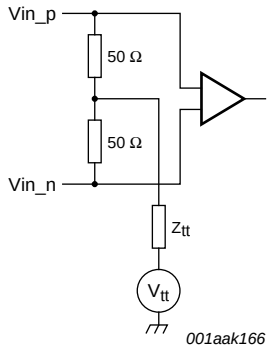


Fig 4. Lane input termination

The common-mode voltage and the termination resistor can be programmed using register HS_RX_RT_VCM (see Table 142) and registers HS_RX_x_RT_REFSIZE (0x12 to 0x16; see Table 144 and Table 145). When not used, the lane input buffer can be set to a High impedance mode (register HS_RX_RT_CTRL; see Table 143).

AC-coupling is always required

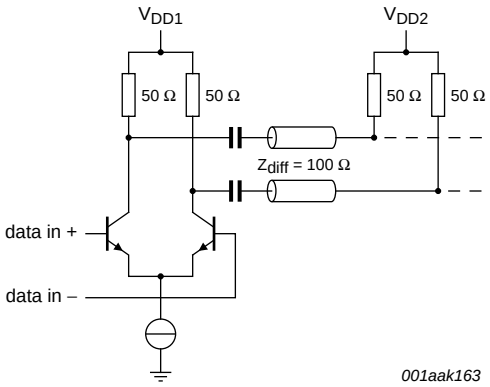


Fig 5. AC-coupling

10.2.2 Equalizer

The DAC1628D1G25 embeds an internal equalizer (bits HS_RX_x_EQ_EN in register HS_RX_EQ_CTRL; see Table 153) in each high-speed serial lane. This improves the interference robustness between signals by amplifying the high-frequency jumps in the data conserving the energy of the low-frequencies ones. The equalizer can be programmed depending on the quality of the channel used (PCB traces/layout, connectors, etc.).

The auto-zero feature (bit HS_RX_EQ_AUTO_ZERO_EN in register HS_RX_EQ_CTRL; see Table 139) is enabled by default for the deserializer to adapt itself to the common-mode of the received signal. This feature can be set manually. It uses an external algorithm that controls the DAC1628D1G25 via the SPI bus.

Set two gains to control the high-frequency and low-frequency jumps of the data (bits HS_RX_x_EQ_HF_GAIN[1:0] and HS_RX_0_EQ_IF_GAIN[2:0] of register HS_RX_x_EQ_GAIN; see Table 140).

10.2.3 Deserializer

The deserializer performs the incoming data clock recovery and also the serial-to-parallel conversion. One global PLL provides the same reference clock to the 4 lanes. Set the PLL using register HS_RX_CDR_DIV (see Table 135).

10.2.4 Synchronization and word alignment

As stated in the JESD204B specification, the transmitter and the receiver first have to synchronize. This is achieved through the SYNC_OUT signals and a synchronization pattern (K28.5 symbol). The receiver (DAC1628D1G25) first drives its SYNC_OUT outputs. The synchronization pattern is continuously sent until the receiver deasserts the SYNC_OUT signal.

The lane processing uses the sync patterns to synchronize the data stream, determine the initial running disparity and extract the 10-bit word from the incoming data stream (word alignment).

The DAC1628D1G25 also uses the SYNC_OUT signal during normal operation to request a link reinitialization when the 10b/8b module loses synchronization.

The SYNC_OUT signal conforms to LVDS signaling. Its common-mode voltage and its single-ended peak amplitude can be programmed using bits SET_SYNC_LVL[3:0] and SYNC_SET_VCM[6:4] in register SYNC_CFG_CTRL (see Table 146).

SYNC_OUT is asynchronous with the frame clock. There is no timing specification of the CLKINP and the CLKINN input, but the DAC1628D1G25 design allows some flexibility in term of the selection of rising edge or falling edge, and a DAC clock period delay.

10.2.5 Comma detection and word alignment

This stage monitors the data stream for code characters (comma detection), decodes the words to bytes (octets) and performs optional character replacement as part of frame/lane alignment monitoring and correction. This module provides the required control signals to the RX controller and ILA.

This module decodes the 10-bit words to 8-bit words (octets). The decoding table is specified in the IEEE 802.3-2005 specification. During decoding, the disparity is calculated according to the disparity rules mentioned in the same specification. The Not-In-Table error (NIT) and Disparity Error (DISP) can be monitored using bits DEC_NIT_ERR_LNx and DEC_DISP_ERR_LNx (register DEC_FLAGS; see Table 93). When the disparity counter is more than +2 or less than −2, an error is generated.

The following comma symbols are detected during data transmission irrespective of the running disparity:

/K/ = K28.5

/F/ = K28.7

/A/ = K28.3

/R/ = K28.0

/Q/ = K28.4

A flag is sent to the control interface to reflect detected commas in registers KOUT_FLAG (see Table 94) and K28_FLAG (see Table 95).

The following flags are also triggered according to the following definitions:

- VALID:

  A code group that is found in the column of the 10b/8b decoding tables according to the current running disparity.
- DISPARITY ERROR:

  The received code group exists in the 10b/8b decoding table, but is not found in the proper column according to the current running disparity.
- NOT-IN-TABLE (NIT) ERROR:

  The received code group is not found in the 10b/8b decoding table for either disparity.
- INVALID:

  A code group that either shows a disparity error or that does not exist in the 10b/8b decoding table.

The DAC1628D1G25 supports character replacement whatever the state of the descrambler. When descrambling is not active (bit DESCR_EN in register ILA_CTRL is set to logic 0; see Table 75), the received K28.3 /A/ or K28.7 /F/ is replaced by the previous sample. When descrambling is active (bit DESCR_EN is set to logic 1), the corresponding data octet D28.3 (0xC) or D28.7 (0xFC) is used.

10.2.6 Descrambler

The descrambler is a 16-bit parallel self-synchronous descrambler based on the polynomial $1 + x^{14} + x^{15}$. This processing can be turned off (bit DESCR_EN in register ILA_CTRL set to logic 0; see Table 75).

10.2.7 Inter-lane alignment

This feature removes strict PCB design skew compensation between the lanes (bits SUP_LN_SYNC, SEL_ILA[1:0], SEL_LOCK[2:0]; see Table 75 and bit DYN_ALIGN_EN; see Table 76).

10.2.7.1 Single device operation

This module handles the alignment of the data streams. Because of inter-lane skew, these alignment characters can be received at different times by the receivers. After the synchronization period, the lock signal is HIGH, enabling the receipt of K28.3 /A/ characters.

The /A/ characters provided in the initial alignment sequence are used to align the data streams. Bits SEL_ILA[1:0] of register ILA_CNTRL (see Table 75) select which K28.3 /A/ symbol triggers the initial lane alignment: 00 = 1st /A/ symbol, 01 = 2nd /A/ symbol, 10 = 3rd /A/ symbol, 11 = 4th /A/ symbol. When all receivers have received their first selected /A/, they start propagating the received data to the frame assembly module at the same point in time (bits SEL_LOCK[2:0]; see Table 75).

This module can compensate up to ±15 character clock period misalignments between the lanes.

If initial lane alignment is not supported, the manual alignment mode can be used (see Table 72 and Table 77).

After the initial ILA sequence, the lane alignment monitoring starts. If the received user data contains a K28.3 /A/ symbol:

- its position is compared to the value of the alignment monitor counter (bit ILA_MON_LNx; see Table 90)
- if two successive K28.3 /A/ symbols have been received at a wrong position, a realignment takes place
- if the buffers are empty or overflow, this is indicated by the registers ILA_BUF_ERR_LN0 to ILA_BUF_ERR_LN3 (see Table 91)

10.2.8 Frame assembly

The DAC1628D1G25 supports the following LMF configuration as described in the JESD204B standard (register LMF_CTRL; see Table 87):

Table 7. LMF configuration

L-M-F	S[1]	HD[2]
1-2-4	1	0
2-2-2	1	0
4-2-2	2	0
4-2-1	1	1

[1] S is the number of samples per frame.

[2] HD is the High-Density bit as described in the JESD204B specification.

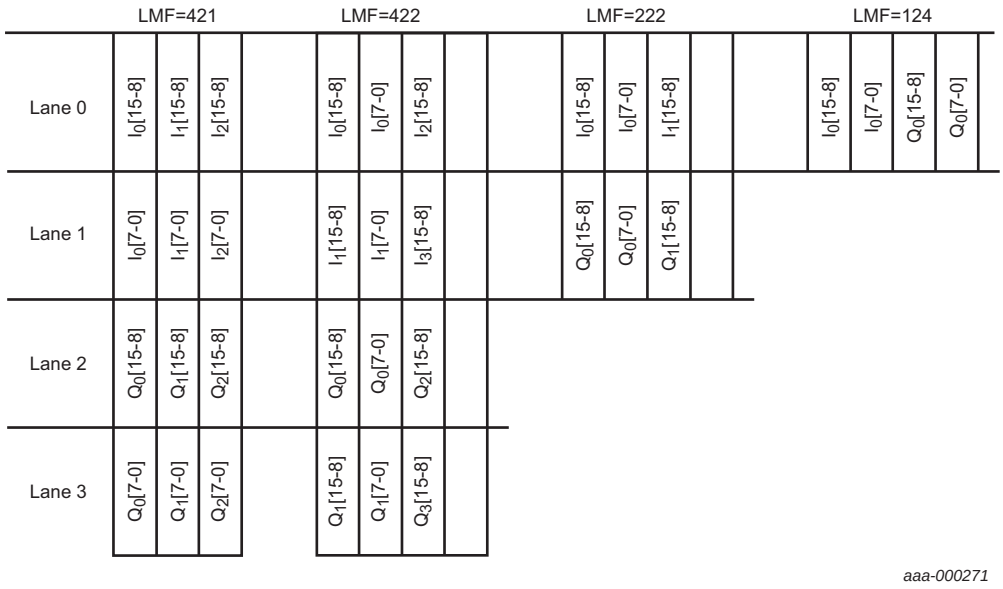


Fig 6. Frame assembly byte representation

10.3 Serial Peripheral Interface (SPI)

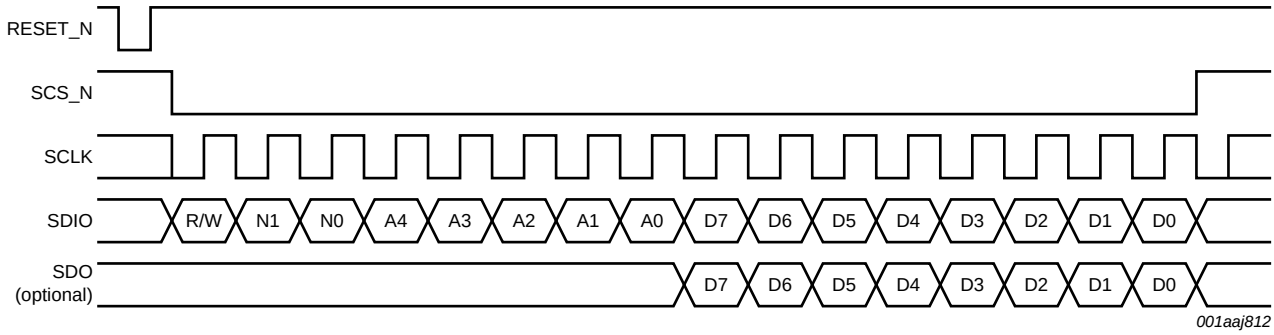
10.3.1 Protocol description

The DAC1628D1G25 serial interface is a synchronous serial communication port allowing easy interfacing with many industry microprocessors. It provides access to the registers that define the operating modes of the chip in both Write mode and Read mode.

This interface can be configured as a 3-wire type (SDIO as bidirectional pin) or a 4-wire type (SDIO and SDO as unidirectional pin, input and output port respectively). In both configurations, SCLK acts as the serial clock and SCS_N acts as the serial chip select.

Each read/write operation is sequenced by the SCS_N signal and enabled by a LOW assertion to drive the chip with 2 bytes to 5 bytes, depending on the content of the instruction byte.

As the DAC1628D1G25 SPI-interface is a slave-device, multiple slave-devices can be attached to the same master interface as long as each device has its own serial chip select signal (SCS_N). The reference voltage of the interface is $V_{DDD(1V8)}$.



R/W indicates the mode access.

The RESET_N signal is not linked to the SPI interface but enable the reset of the registers to the default values.

Fig 7. SPI protocol

Table 8. Read or Write mode access description

R/W	Description
0	Write mode operation
1	Read mode operation

In Table 9, N1 and N0 indicate the number of bytes transferred after the instruction byte.

Table 9. Number of bytes transferred

N1	N0	Number of bytes transferred
0	0	1
0	1	2
1	0	3
1	1	4

A[4:0] indicates which register is being addressed. If a multiple transfer occurs, this address points to the first register to be accessed. The address is then internally decreased after each following data phase.

10.3.2 SPI timing description

The SPI interface can operate at a frequency of up to 15 MHz. Figure 8 shows the SPI timing.

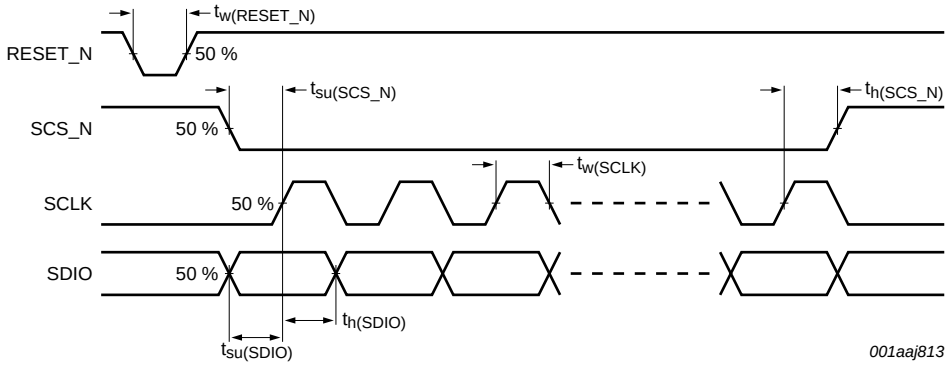


Fig 8. SPI timing diagram

The SPI timing characteristics are given in the following table.

Table 10. SPI timing characteristics

Symbol	Parameter		Min	Typ	Max	Unit
f_{SCLK}	SCLK frequency		-	-	15	MHz
$t_{w(SCLK)}$	SCLK pulse width		30	-	-	ns
$t_{su(SCS\_N)}$	SCS_N set-up time		20	-	-	ns
$t_{h(SCS\_N)}$	SCS_N hold time		20	-	-	ns
$t_{su(SDIO)}$	SDIO set-up time		10	-	-	ns
$t_{h(SDIO)}$	SDIO hold time		5	-	-	ns
$t_{w(RESET\_N)}$	RESET_N pulse width	[1]	30	-	-	ns

[1] The RESET_N signal is not linked to the SPI interface but enable the reset of the registers to the default values.

10.4 Clock input

The DAC1628D1G25 incorporates one differential clock input, CLKINN/CLKINP.

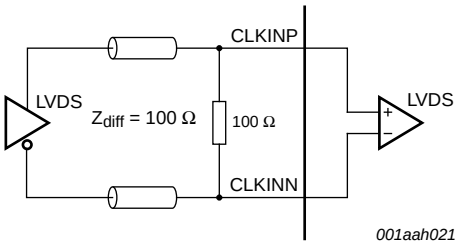


Fig 9. LVDS clock configuration

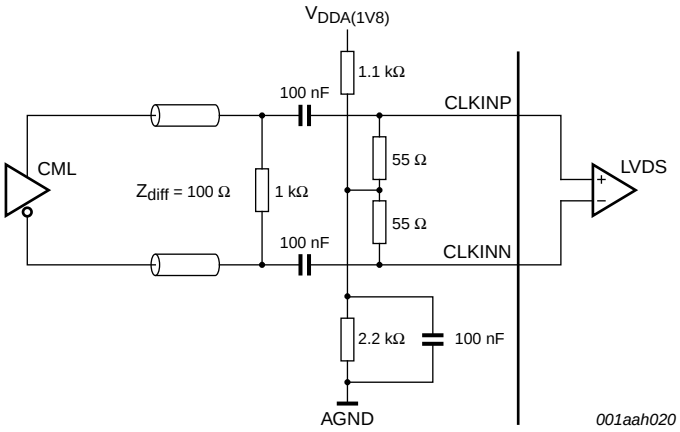


Fig 10. Interfacing CML to LVDS

The DAC1628D1G25 can operate with a clock frequency up to 500 MHz, or up to 1250 MHz if the internal PLL is bypassed. The clock input can be LVDS but it can also be interfaced with CML. Clock Domain Interface (CDI) logic handles the error free data transition from one internal clock domain to another.

During the reset phase (RESET_N asserted), the clock must be stable and running, ensuring a proper reset of the complete device.

10.5 Operating modes

The DAC1628D1G25 requires one single differential clock: the data clock (CLKINP, CLKINN) for the internal PLL and the dual DAC core.

Set CDI and PLL correctly to configure the DAC1628D1G25 for application mode.

10.6 Finite Impulse Response (FIR) filters

The three interpolation FIR filters have a stop band attenuation of at least 80 dBc and a pass band ripple of less than 0.0005 dB.

Table 11. Interpolation filter coefficients

First interpolation filter			Second interpolation filter			Third interpolation filter		
Lower	**Upper**	**Value**	**Lower**	**Upper**	**Value**	**Lower**	**Upper**	**Value**
H(1)	H(55)	−4	H(1)	H(23)	−2	H(1)	H(15)	−39
H(2)	H(54)	0	H(2)	H(22)	0	H(2)	H(14)	0
H(3)	H(53)	+13	H(3)	H(21)	+17	H(3)	H(13)	+273
H(4)	H(52)	0	H(4)	H(20)	0	H(4)	H(12)	0
H(5)	H(51)	−34	H(5)	H(19)	−75	H(5)	H(11)	−1102
H(6)	H(50)	0	H(6)	H(18)	0	H(6)	H(10)	0
H(7)	H(49)	+72	H(7)	H(17)	+238	H(7)	H(9)	+4964
H(8)	H(48)	0	H(8)	H(16)	0	H(8)	-	+8192
H(9)	H(47)	−138	H(9)	H(15)	−660	-	-	-
H(10)	H(46)	0	H(10)	H(14)	0	-	-	-

Table 11. Interpolation filter coefficients

First interpolation filter			Second interpolation filter			Third interpolation filter		
Lower	Upper	Value	Lower	Upper	Value	Lower	Upper	Value
H(11)	H(45)	+245	H(11)	H(13)	+2530	-	-	-
H(12)	H(44)	0	H(12)	-	+4096	-	-	-
H(13)	H(43)	–408	-	-	-	-	-	-
H(14)	H(42)	0	-	-	-	-	-	-
H(15)	H(41)	+650	-	-	-	-	-	-
H(16)	H(40)	0	-	-	-	-	-	-
H(17)	H(39)	–1003	-	-	-	-	-	-
H(18)	H(38)	0	-	-	-	-	-	-
H(19)	H(37)	+1521	-	-	-	-	-	-
H(20)	H(36)	0	-	-	-	-	-	-
H(21)	H(35)	–2315	-	-	-	-	-	-
H(22)	H(34)	0	-	-	-	-	-	-
H(23)	H(33)	+3671	-	-	-	-	-	-
H(24)	H(32)	0	-	-	-	-	-	-
H(25)	H(31)	–6642	-	-	-	-	-	-
H(26)	H(30)	0	-	-	-	-	-	-
H(27)	H(29)	+20756	-	-	-	-	-	-
H(28)	-	+32768	-	-	-	-	-	-

10.7 Single-Side Band Modulator (SSBM)

The single-side band modulator is a quadrature modulator that enables the mixing of the I data and Q data with the sine and cosine signals generated by the NCO to generate path A and B as described in Figure 11.

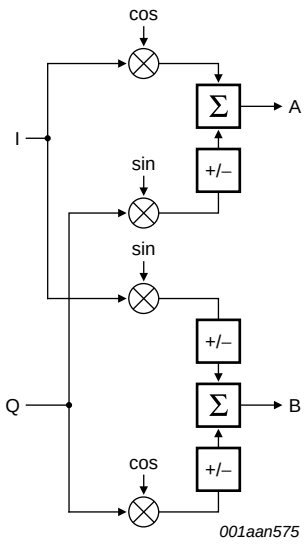


Fig 11. Single-side band modulator principle

Table 12 shows the various possibilities set by register MODULATION (see Table 19).

Table 12. Complex modulator operation mode

MODULATION[2:0]	Mode	Path A	Path B
000	bypass	$I(t)$	$Q(t)$
001	positive upper ssb	$I(t) \times cos(\omega_{NCO} \times t) - Q(t) \times sin(\omega_{NCO} \times t)$	$I(t) \times sin(\omega_{NCO} \times t) + Q(t) \times cos(\omega_{NCO} \times t)$
010	positive lower ssb	$I(t) \times cos(\omega_{NCO} \times t) + Q(t) \times sin(\omega_{NCO} \times t)$	$I(t) \times sin(\omega_{NCO} \times t) - Q(t) \times cos(\omega_{NCO} \times t)$
011	negative upper ssb	$I(t) \times cos(\omega_{NCO} \times t) - Q(t) \times sin(\omega_{NCO} \times t)$	$-I(t) \times sin(\omega_{NCO} \times t) - Q(t) \times cos(\omega_{NCO} \times t)$
100	negative lower ssb	$I(t) \times cos(\omega_{NCO} \times t) + Q(t) \times sin(\omega_{NCO} \times t)$	$-I(t) \times sin(\omega_{NCO} \times t) + Q(t) \times cos(\omega_{NCO} \times t)$
others	not defined	-	-

10.7.1 40-bit NCO

When using the NCO, the 5 registers FREQNCO_B0 to FREQNCO_B4 over 40 bits (see Table 21) can set the frequency.

The frequency is calculated with Equation 1:

$$f_{NCO} = \frac{M \times f_s}{2^{40}} \quad (1)$$

Where:

- M is the value set in the bits FREQNCO[39:0] of the NCO frequency registers (see Table 21).
- f_s is the DAC output clock sampling frequency

The registers PHINCO_LSB and PHINCO_MSB over 16 bits from 0° to 360° (see Table 20) can set the phase of the NCO.

The default settings represent an NCO frequency of 96 MHz when using a DAC clock of 640 Msps. For other DAC clock frequencies, use Equation 1 to define the associated NCO frequency.

10.7.2 NCO low power

When using NCO low power (bit NCO_LP_SEL; see Table 19), the five most significant bits of register FREQNCO_B4 (bits FREQ_NCO[39:32]; see Table 21) can set the frequency.

The frequency is calculated with Equation 2:

$$f_{NCO} = \frac{M \times f_s}{2^{40}} \quad (2)$$

Where:

- M is the value set in the bits FREQNCO[39:0] of the NCO frequency registers (see Table 21).
- f_s is the DAC clock sampling frequency

The eight most significant bits of the NCO phase offset registers (PH_NCO[7:0]; see Table 20) can set the phase of the NCO low power.

10.7.3 Minus 3dB

In normal use, a full-scale pattern is also full-scale at the DAC output. Nevertheless, when the I data and Q data come close to full-scale simultaneously, some clipping can occur. The Minus 3dB function (bit MINUS_3DB of register DAC_OUT_CTRL; see Table 24) can be used to reduce the 3 dB gain in the modulator. It retains a full-scale range at the DAC output without added interferers.

10.8 Inverse sinx / x

A selectable FIR filter is incorporated to compensate the sinx / x effect caused by the roll-off effect of the DAC. The coefficients are represented in Table 13.

Table 13. Inversion filter coefficients

First interpolation filter		
Lower	**Upper**	**Value**
H(1)	H(9)	+1
H(2)	H(8)	–4
H(3)	H(7)	+13
H(4)	H(6)	–51
H(5)	-	+610

Remark: The transfer function of this features adds some gain to the signals and some clipping can occur with a level of distortion in the output spectrum as result. Update the digital gain accordingly to avoid this clipping.

10.9 DAC transfer function

The full-scale output current for each DAC is the sum of the two complementary current outputs:

- $I_{OA(fs)} = I_{IOUTAP} + I_{IOUTAN}$
- $I_{OB(fs))} = I_{IOUTBP} + I_{IOUTBN}$

The output current of DAC A depends on the digital input data and the gain factor defined by bits DAC_A_GAIN[11:0] of register DAC_A_DGAIN_MSB (see Table 23).

$$I_{IOUTAP} = I_{OA(fs)} \times \frac{(DAC\_A\_DGAIN)}{1024} \times \left(\frac{DATA}{(65535)}\right) \quad (3)$$

$$I_{IOUTAN} = I_{OA(fs)} \times \left(1 - \frac{(DAC\_A\_DGAIN)}{1024} \times \left(\frac{DATA}{(65535)}\right)\right) \quad (4)$$

The output current of DAC B depends on the digital input data and the gain factor defined by bits DAC_B_DGAIN[11:0] of register DAC_B_DGAIN_LSB (see Table 23).

$$I_{IOUTBP} = I_{OB(fs)} \times \frac{(DAC\_B\_DGAIN)}{1024} \times \left(\frac{DATA}{(65535)}\right) \quad (5)$$

$$I_{IOUTBN} = I_{OB(fs)} \times \left(1 - \frac{(DAC\_B\_DGAIN)}{1024} \times \left(\frac{DATA}{(65535)}\right)\right) \quad (6)$$

It is possible to define if the DAC1628D1G25 operates with a binary input or a two's complement input (bit CODING; see Table 18).

Table 14 shows the output current as a function of the input data, when $I_{OA(fs)} = I_{OB(fs)} = 20$ mA.

Table 14. DAC transfer function

Data	I15 to I0/Q15 to Q0 (binary coding)	I15 to I0/Q15 to Q0 (two's complement coding	IOUTAP/IOUTBP	IOUTAN/IOUTBN
0	0000 0000 0000 0000	1000 0000 0000 0000	0 mA	20 mA
...	...	...	...	....
32768	1000 0000 0000 0000	0000 0000 0000 0000	10 mA	10 mA
...	...	...	...	...
65535	1111 1111 1111 1111	0111 1111 1111 1111	20 mA	0 mA

10.10 Full-scale current

10.10.1 Regulation

The DAC1628D1G25 reference circuitry integrates an internal band gap reference voltage which delivers a 1.25 V reference on the GAPOUT pin. Decouple pin GAPOUT using a 100 nF capacitor.

The reference current is generated via an external resistor of 910 Ω (1 %) connected to VIRES. A control amplifier sets the appropriate full-scale current ($I_{OA(fs)}$ and $I_{OB(fs)}$) for both DACs (bits DAC_A_GAIN[9:0] (see Table 41).

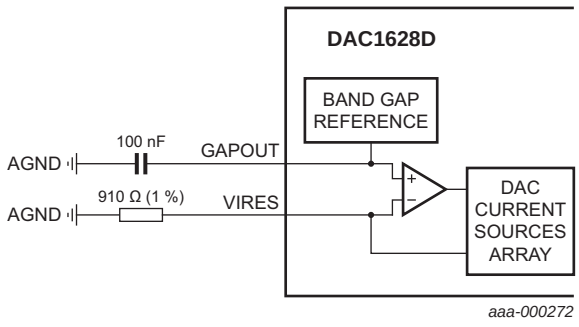


Fig 12. Internal reference configuration

Figure 12 shows the optimal configuration for temperature drift compensation because the band gap reference voltage can be matched to the voltage across the feedback resistor.

The DAC current can also be adjusted by applying an external reference voltage to the non-inverting input pin GAPOUT and disabling the internal band gap reference voltage (bit GAP_PON; see Table 18).

10.10.2 Full-scale current adjustment

The default full-scale current ($I_{O(fs)}$) is 20 mA but further adjustments can be made to both DACs independently via the serial interface from 8.1 mA to 34 mA.

The settings applied to DAC_A_GAIN[9:0] (see Table 21) define the full-scale current of DAC A:

$$I_{O(fs)}\ (\mu A) = 8100 + \text{DAC\_A\_GAIN}[9:0] \times 25.3 \quad (7)$$

The DAC_B_GAIN[9:0] (see Table 21) define the full-scale current of DAC B:

$$I_{O(fs)}\ (\mu A) = 8100 + \text{DAC\_B\_GAIN}[9:0] \times 25.3 \quad (8)$$

10.11 Digital offset adjustment

When the DAC1628D1G25 analog output is DC connected to the next stage, the digital offset correction (bits DAC_A_OFFSET[15:0] and DAC_B_OFFSET[15:0]; see Table 26) can be used to adjust the common-mode level at the output of each DAC. It adds an offset at the end of the digital part, just before the DACs. Following table shows the range of variation of the digital offset.

Table 15. Digital offset adjustment

DAC_A_OFFSET[15:0] DAC_B_OFFSET[15:0] (two's complement)	Offset applied
1000 0000 0000 0000	–32768
1000 0000 0000 0001	–32767
...	...
1111 1111 1111 1111	–1
0000 0000 0000 0000	0
0000 0000 0000 0001	+1
...	...
0111 1111 1111 1110	+32766
0111 1111 1111 1111	+32767

10.12 Analog output

The device has two output channels, each producing two complementary current outputs, which enable the reduction of even-order harmonics and noise. The pins are IOUTAP/IOUTAN and IOUTBP/IOUTBN. Connect these pins using a load resistor R_L to the 3.3 V analog power supply ($V_{DDA(3V3)}$).

Figure 13 shows the equivalent analog output circuit of one DAC. This circuit includes a parallel combination of NMOS current sources and associated switches for each segment.

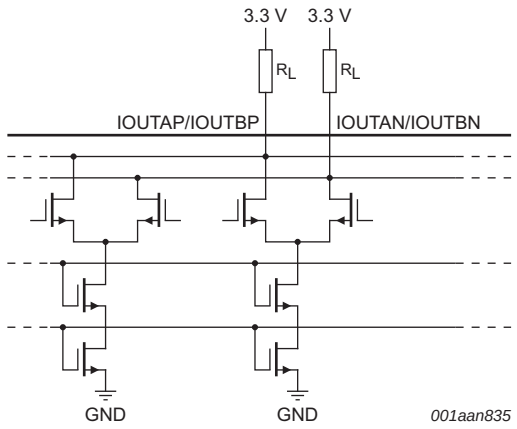


Fig 13. Equivalent analog output circuit

The cascode source configuration increases the output impedance of the source, which improves the dynamic performance of the DAC because there is less distortion.

Depending on the application, the various stages and the targeted performances, the device can be used for an output level of up to 2 V (p-p).

10.13 Auxiliary DACs

The DAC1628D1G25 integrates two auxiliary DACs, which are used to compensate any offset between the DACs and the next stage in the transmission path. Both auxiliary DACs have a 10-bit resolution and are current sources (referenced to ground).

The full-scale output current for each DAC is the sum of the two complementary current outputs:

- $I_{OAUXA(fs)} = I_{AUXAP} + I_{AUXAN}$
- $I_{OAUXB(fs)} = I_{AUXBP} + I_{AUXBN}$

The output current depends on the digital input data set by SPI registers DAC_A_AUX_MSB (bits AUX_A[9:2]), DAC_A_AUX_LSB (bits AUX_A[1:0]), DAC_B_AUX_MSB (bits AUX_B[9:2]) and DAC_B_AUX_LSB (bits AUX_B[1:0]; see Table 42).

$$I_{AUXAP} = I_{OAUXA(fs)} \times \left(\frac{DATAA}{1023}\right) \quad (9)$$

$$I_{AUXAN} = I_{OAUXA(fs)} \times \left(\frac{1023 - DATAA}{1023}\right) \quad (10)$$

$$I_{AUXBP} = I_{OAUXB(fs)} \times \left(\frac{DATAB}{1023}\right) \quad (11)$$

$$I_{AUXBN} = I_{OAUXB(fs)} \times \left(\frac{1023 - DATAB}{1023}\right) \quad (12)$$

Table 16 shows the output current as a function of the auxiliary DACs data DATAA and DATAB Equation 9 to Equation 12.

Table 16. Auxiliary DAC transfer function

DATAA; DATAB	AUX_A[9:2]/AUX_A[1:0]; AUX_B[9:0]/AUX_B[1:0] (binary coding)	I_{AUXAP}; I_{AUXBP} (mA)	I_{AUXAN}; I_{AUXBN} (mA)
0	00 0000 0000	0	2.2
...	...	...	...
512	10 0000 0000	1.1	1.1
...	...	...	...
1023	11 1111 1111	2.2	0

10.14 Phase correction

The IQ-modulator which follows the DACs can have a phase imbalance which results in undesired sidebands. By adjusting the phase between the I and Q channels, the spur can be reduced.

Without compensation the I and Q have a phase difference of π / 2 (90°). The registers PH_CORR_CTRL0 and PH_CORR_CTRL1(see Table 22) ensure a phase variation from 75.7° to 104.3°. The two registers define a signed value that ranges from −2048 to +2048. the equation: PH_CORR[12:0] / 16384 gives the resulting phase compensation (in radians).

10.15 Output configuration

10.15.1 Basic output configuration

Using a differentially coupled transformer output (see Figure 14) provides optimum distortion performance. In addition, it helps to match the impedance and provides electrical isolation.

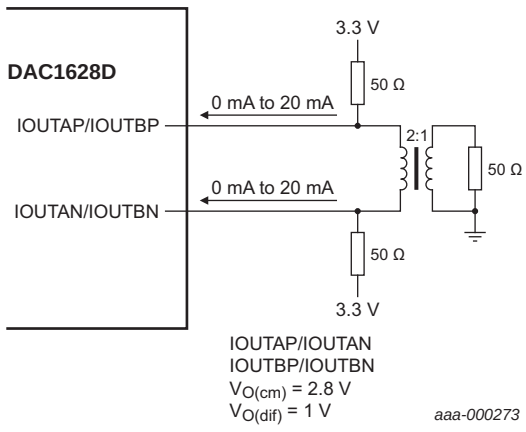


Fig 14. 1 V (p-p) differential output with transformer

The DAC1628D1G25 can operate a differential output of up to 2 V (p-p). In this configuration, connect the center tap of the transformer to a 62 Ω resistor, which is connected to the 3.3 V analog power supply. This adjusts the DC common-mode to around 2.7 V (see Figure 15).

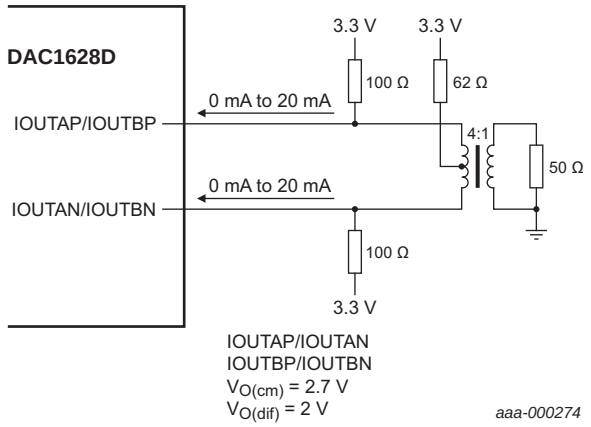


Fig 15. 2 V (p-p) differential output with transformer

10.15.2 IQ-modulator - BGX7100 interface

The DAC1628D1G25 can be easily connected to the BGX7100 NXP IQ-modulator. The offset compensation for local oscillator can be canceled using the digital offset control in the device. The DAC digital gain and phase compensation can also be used to cancel the image.

Figure 16 shows an example of a connection between the DAC1628D1G25 and the BGX7100 interface.

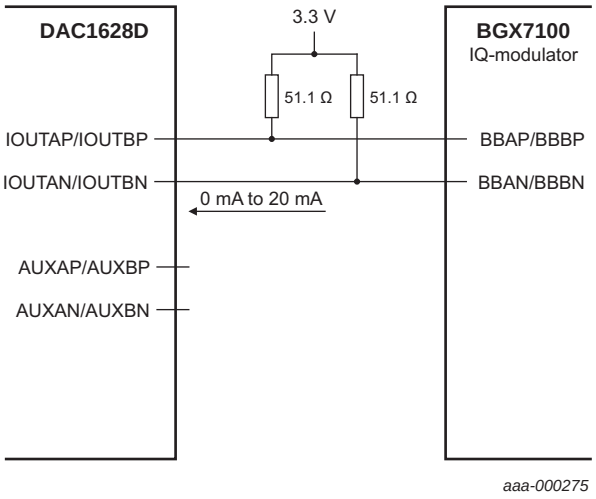


Fig 16. DAC1628D1G25 with BGX7100 IQ-modulator interface

10.15.3 IQ-modulator - DC interface

When the system operation requires to keep the DC component of the spectrum, the DAC1628D1G25 can use a DC interface to connect an IQ-modulator. In this case, the offset compensation for local oscillator can be canceled using the digital offset control in the device.

Figure 17 shows an example of a connection to an IQ modulator with a 1.7 V common input level.

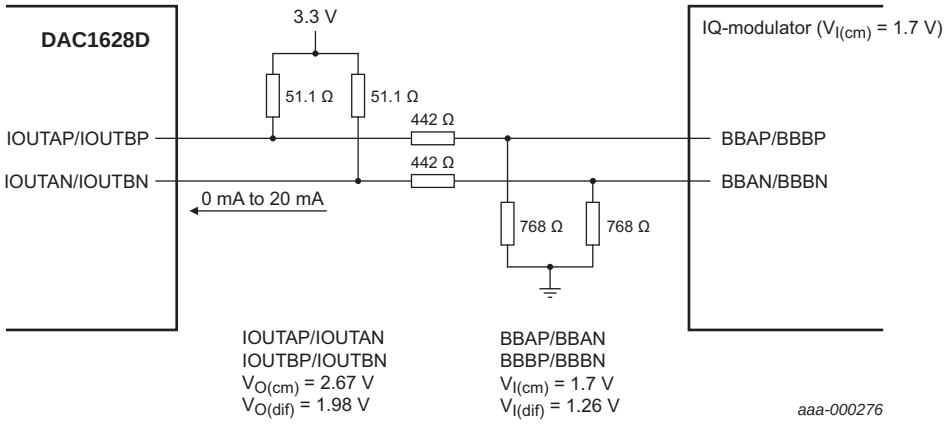


Fig 17. IQ-modulator: DC interface with a 1.7 V common input level

Figure 18 shows an example of a connection to an IQ-modulator with a 3.3 V common input level.

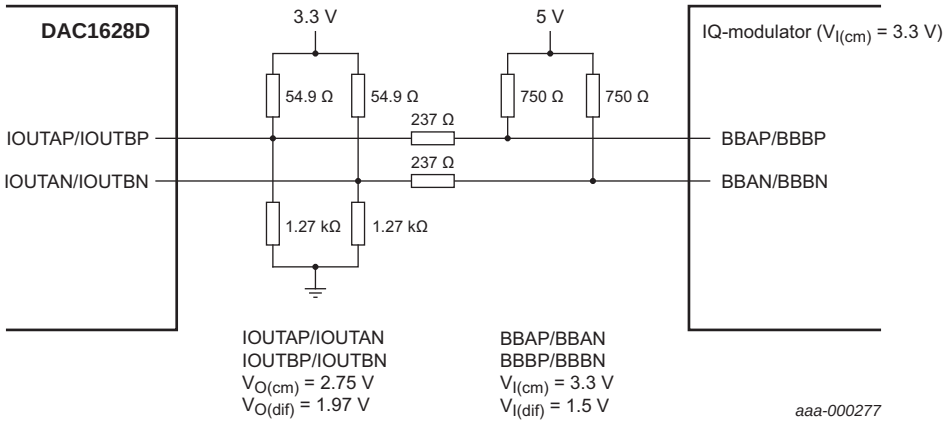


Fig 18. IQ-modulator: DC interface with a 3.3 V common input level

The auxiliary DACs can be used to control the offset within an accurate range or with accurate steps.

Figure 19 shows an example of a connection to an IQ-modulator with a 1.7 V common input level and auxiliary DACs.

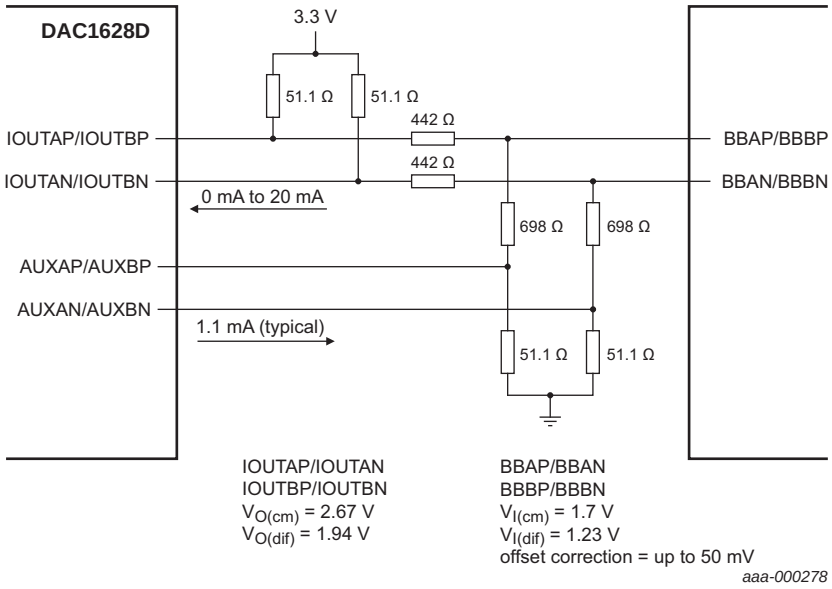


Fig 19. IQ-modulator: DC interface with a 1.7 V common input level and auxiliary DACs

Figure 20 shows an example of a connection to an IQ-modulator with a 3.3 V common input level and auxiliary DACs.

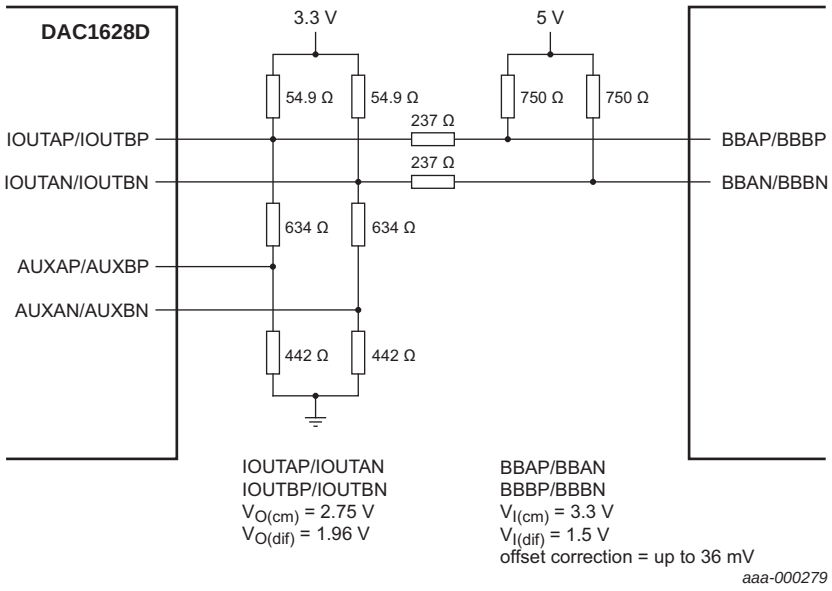


Fig 20. IQ-modulator: DC interface with a 3.3 V common input level and auxiliary DACs

The constraints to adjust the interface are:

- The output compliance range of the DAC
- The output compliance range of the auxiliary DACs
- The input common-mode level of the IQ-modulator
- The range of offset correction

10.15.4 IQ-modulator - AC interface

Use the DAC1628D1G25 AC-coupled when the IQ-modulator common-mode voltage is close to ground. The auxiliary DACs are required for local oscillator cancelation.

Figure 21 shows an example of a connection to an IQ-modulator with a 0.5 V common input level and auxiliary DACs.

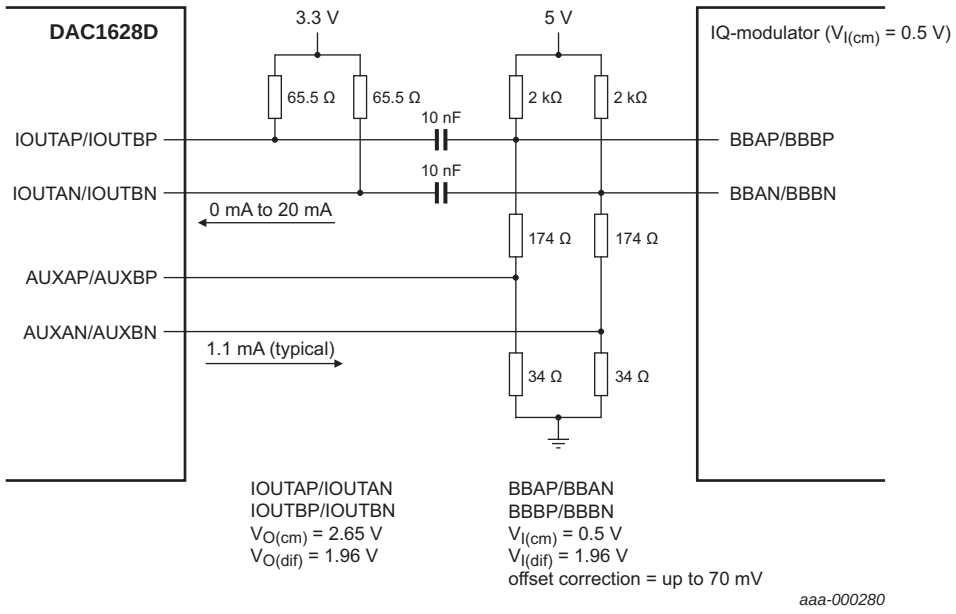


Fig 21. IQ-modulator: AC interface with a 0.5 V common input level and auxiliary DACs

10.16 Design recommendations

10.16.1 Power and grounding

Use a separate power supply regulator for the generation of the 1.8 V analog power (pins 43, 48. 51. 56) and the 1.8 V digital power (pins 7, 10, 33, 36) to ensure optimal performance.

High-speed input lanes are powered by a 1.8 V power supply that can require a dedicated power supply. Pins 15, 16, 19, 22, 25, 28 can be connected to either the global 1.8 V power supply or to a dedicated one.

Also, include individual LC decoupling for the following six sets of power pins:

- $V_{DDA(1V8)}$ (pins 43, 46, 48, 51, 53 and 56)
- $V_{DDD(1V8)}$ (core: pins 7, 10, 15, 16, 19, 22, 25, 28, 33 and 36)
- $V_{DDA(3V3)}$ (pins 47 and 52)

Use at least two capacitors for each power pin decoupling. Locate these capacitors as close as possible to the DAC1628D1G25 power pins.

Use a separate LDO for the generation of the 1.8 V analog power ($V_{DDA(1V8)}$ and the 1.8 V digital power (V_{DDD1V8}) to ensure the best performance.

The die pad is used for both the power dissipation and electrical grounding. Insert several vias (typically 7×7 to connect the internal ground plane to the top layer die area.

10.17 Registers

Figure 22 shows an overview of all register pages.

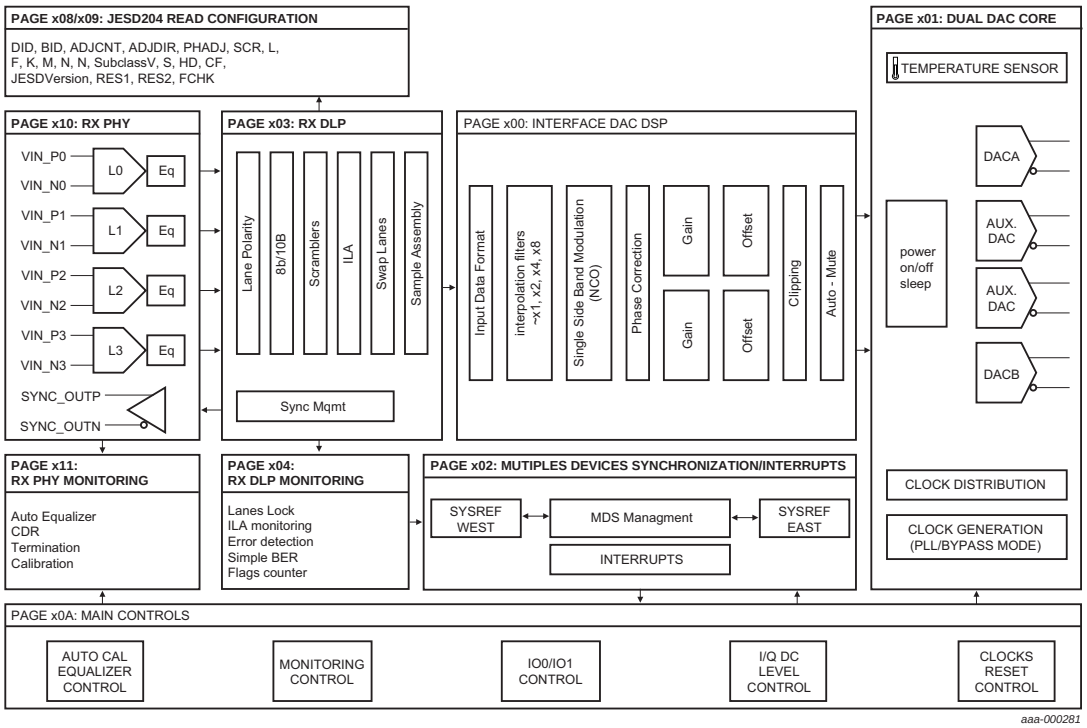


Fig 22. SPI register pages repartition

10.17.1 Page x00: Interface DAC DSP

This page specifies the main features of the digital signal processing of the DAC1628D1G25.

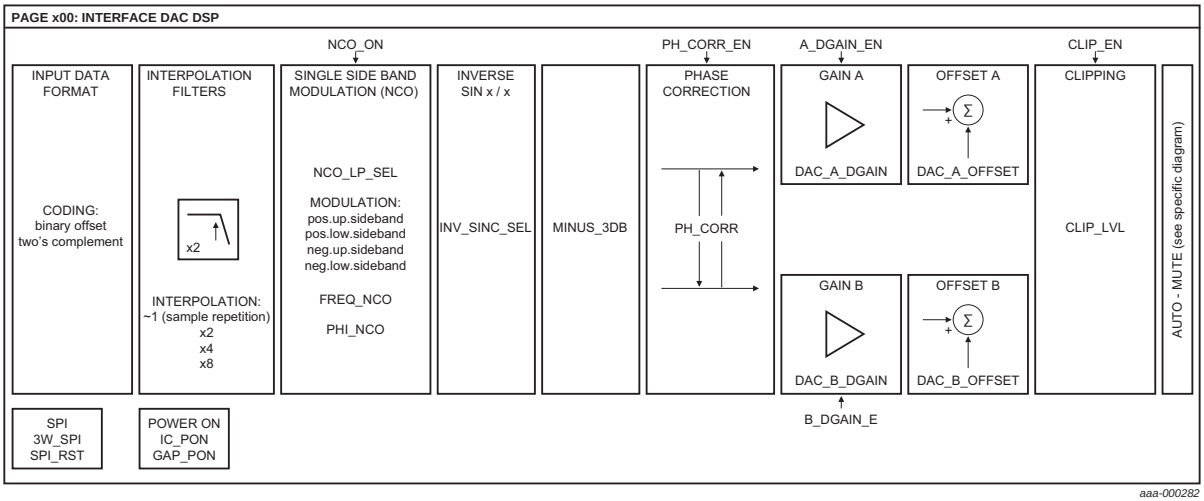


Fig 23. Page x00, interface DAC DSP overview

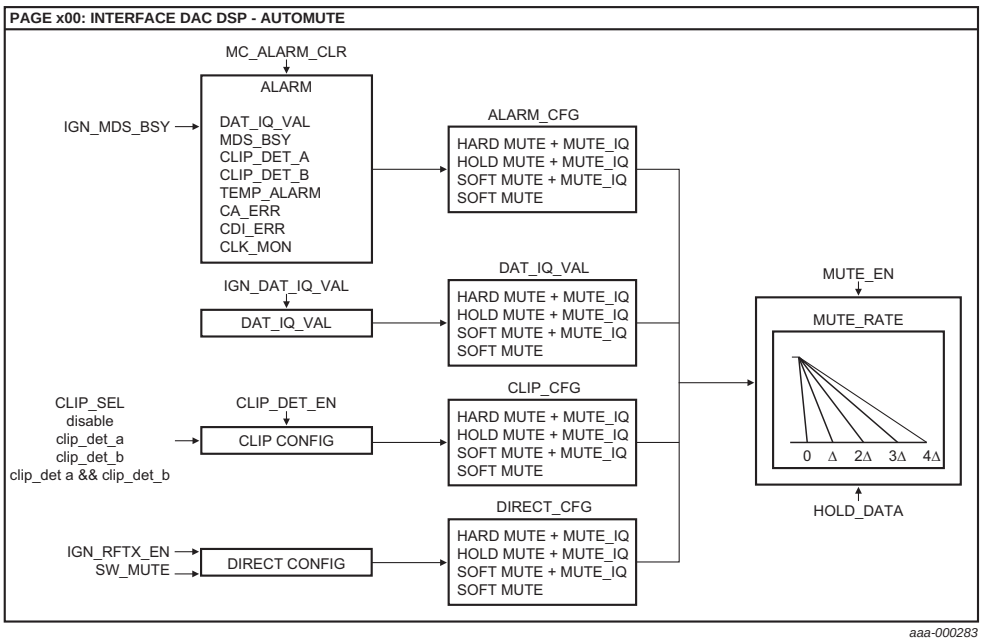


Fig 24. Page x00, Automute

10.17.1.1 Page x00 - register allocation map

Table 17 shows an overview of all registers on page x00.

Table 17. Page x00 register allocation map

Address		Register name	R/W	Bit definition								Default	
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
0	00h	COMMON	R/W	3W_SPI	SPI_RST	-	-	-	CODING	IC_PON	GAP_PON	1000 0111	87h
1	01h	TXCFG	R/W	NCO_ON	NCO_LP_SEL	INV_SINC_SEL	MODULATION[2:0]			INTERPOLATION[1:0]		0000 0001	01h
2	02h	PHINCO_LSB	R/W	PHI_NCO[7:0]								0000 0000	00h
3	03h	PHINCO_MSB	R/W	PHI_NCO[15:8]								0000 0000	00h
4	04h	FREQ_NCO_B0	R/W	FREQ_NCO[7:0]								0110 0110	66h
5	05h	FREQ_NCO_B1	R/W	FREQ_NCO[15:8]								0110 0110	66h
6	06h	FREQ_NCO_B2	R/W	FREQ_NCO[23:16]								0110 0110	66h
7	07h	FREQ_NCO_B3	R/W	FREQ_NCO[31:24]								0010 0110	66h
8	08h	FREQ_NCO_B4	R/W	FREQ_NCO[39:32]								0010 0110	26h
9	09h	PH_CORR_CTRL0	R/W	PH_CORR[7:0]								0000 0000	00h
10	0Ah	PH_CORR_CTRL1	R/W	PH_COR_EN	-	-	PH_COR[12:8]					0000 0000	00h
11	0Bh	DAC_A_DGAIN_LSB	R/W	DAC_A_DGAIN[7:0]								1101 0100	50h
12	0Ch	DAC_A_DGAIN_MSB	R/W	-	-	-	-	DAC_A_DGAIN[11:8]				0000 1011	0Bh
13	0Dh	DAC_B_DGAIN_LSB	R/W	DAC_B_DGAIN[7:0]								1101 0100	50h
14	0Eh	DAC_B_DGAIN_MSB	R/W	-	-	-	-	DAC_B_DGAIN[11:8]				0000 0010	0Bh

Table 17. Page x00 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default	
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
15	0Fh	DAC_OUT_CNTRL	R/W	-	-	-	-	A_DGAIN_EN	B_DGAIN_EN	MINUS_3DB	CLIP_EN	0000 0000	00h
16	10h	DAC_CLIPPING	R/W	CLIP_LVL[7:0]								1111 1111	FFh
17	11h	DAC_A_OFFSET_LSB	R/W	DAC_A_OFFSET[7:0]								0000 0000	00h
18	12h	DAC_A_OFFSET_MSB	R/W	DAC_A_OFFSET[15:8]								0000 0000	00h
19	13h	DAC_B_OFFSET_LSB	R/W	DAC_B_OFFSET[7:0]								0000 0000	00h
20	14h	DAC_B_OFFSET_MSB	R/W	DAC_B_OFFSET[15:8]								0000 0000	00h
21	15h	MUTE_CNTRL_0	R/W	HOLD_DATA	CLIP_SEL[1:0]		CLIP_DET_EN	MUTE_EN	MUTE_RATE[2:0]			0000 0100	04h
22	16h	MUTE_CNTRL_1	R/W	ALARM_CFG[1:0]		DAT_V_IQ_CFG[1:0]		CLIP_CFG[1:0]		DIRECT_CFG[1:0]		0001 1011	00h
23	17h	MUTE_CNTRL_2	R/W	MC_ALARM_CLR	IGN_RFTX_EN	IGN_MDS_BSY	IGN_DAT_IQ_VAL	-	-	-	SW_MUTE	0000 0000	00h
24	18h	MUTE_AL_EN	R/W	DAT_IQ_VAL	MDS_BSY	CLIP_DET_A	CLIP_DET_B	TEMP_ALARM	CA_ERR	MON_DCLK_ERR	CLK_MON	0000 0000	00h
25	19h	PAGE_ADDRESS	R/W	-	-	-	PAGE[4:0]					0000 0000	00h

10.17.1.2 Page x00 bit definition detailed description

The tables in this section contain detailed descriptions of the page x00 registers.

Table 18. Register COMMON (address 00h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7	3W_SPI	R/W		serial interface bus type
			0	4-wire SPI
			1	**3-wire SPI**
6	SPI_RST	R/W		serial interface reset
			0	**no reset**
			1	performs a reset on all registers except address 00h
2	CODING	R/W		coding of input word
			0	two's complement coding
			1	**unsigned format**
1	IC_PON	R/W		IC power control
			0	all circuits (digital and analog, except SPI) are in power-down
			1	**all circuits (digital and analog, except SPI) are switched on**
0	GAP_PON	R/W		internal band gap power control
			0	band gap is power-down
			1	**internal band gap references are switched on**

Table 19. Register TXCFG (address 01h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7	NCO_ON	R/W		NCO
			0	**NCO disabled, the NCO phase is reset to 0**
			1	NCO enabled
6	NCO_LP_SEL	R/W		NCO low power selection
			0	**low power NCO disabled**
			1	low power NCO enabled (frequency and phase given by the five MSB of the registers 06h and 08h, respectively)
5	INV_SIN_SEL	R/W		inverse (sin x) / x function selection
			0	**disabled**
			1	enabled
4 to 2	MODULATION[2:0]	R/W		modulation
			000	**dual DAC: no modulation**
			001	positive upper single sideband upconversion
			010	positive lower single sideband upconversion
			011	negative upper single sideband upconversion
			100	negative lower single sideband upconversion
			others	not defined

Table 19. Register TXCFG (address 01h) bit description *...continued*

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
1 to 0	INTERPOLATION[1:0]	R/W		interpolation
			00	no interpolation
			01	**×2 interpolation**
			10	×4 interpolation
			11	×8 interpolation

Table 20. NCO phase offset registers (address 02h to 03h) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
02h	PHINCO_LSB	7 to 0	PH_NCO[7:0]	R/W	-	least significant 8 bits for the NCO phase offset
03h	PHINCO_MSB	7 to 0	PH_NCO[15:8]	R/W	-	most significant 8 bits for the NCO phase offset

Table 21. NCO frequency registers (address 04h to 08h) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
04h	FREQNCO_B0	7 to 0	FREQNCO[7:0]	R/W		NCO frequency
					-	least significant 8 bits for the NCO frequency setting
05h	FREQNCO_B1	7 to 0	FREQNCO[15:8]		-	intermediate 8 bits for the NCO frequency setting
06h	FREQNCO_B2	7 to 0	FREQNCO[23:16]		-	intermediate 8 bits for the NCO frequency setting
07h	FREQNCO_B3	7 to 0	FREQNCO[31:24]		-	intermediate 8 bits for the NCO frequency setting
08h	FREQNCO_B4	7 to 0	FREQNCO[39:32]		-	most significant 8 bits for the NCO frequency setting

Table 22. DAC output phase correction factor registers (address 09h to 0Ah) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
09h	PH_CORR_CTRL0	7 to 0	PH_CORR[7:0]	R/W		DAC output phase correction factor (LSB)
					-	least significant 8 bits for the DAC output phase correction factor
0Ah	PH_CORR_CTRL1	7	PH_CORR_EN	R/W		DAC output phase correction control
					0	**DAC output phase correction disabled**
					1	DAC output phase correction enabled
		4 to 0	PH_CORR[12:8]			DAC output phase correction factor MSB
					00000	most significant 5 bits for the DAC output phase correction factor

Table 23. DAC digital gain control registers (address 0Bh to 0Eh) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0Bh	DAC_A_DGAIN_LSB	7 to 0	DAC_A_DGAIN[7:0]	R/W		DAC A digital gain control
					-	least significant 8 bits for DAC A digital gain
0Ch	DAC_A_DGAIN_MSB	3 to 0	DAC_A_DGAIN[11:8]		-	most significant 4 bits for DAC A digital gain
0Dh	DAC_B_DGAIN_LSB	7 to 0	DAC_B_DGAIN[7:0]	R/W		DAC B digital gain control
					-	least significant 8 bits for DAC B digital gain
0Eh	DAC_B_DGAIN_MSB	3 to 0	DAC_B_DGAIN[11:8]		-	most significant 4 bits for DAC B digital gain

Table 24. Register DAC_OUT_CTRL (address 0Fh)

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
3	DAC_A_GAIN_EN	R/W		DAC A digital gain control
			0	**disable**
			1	enable
2	DAC_B_GAIN_EN	R/W		DAC B digital gain control
			0	**disable**
			1	enable
1	MINUS_3DB	R/W		DAC attenuation control
			0	**unity gain**
			1	−3 dB gain
0	CLIP_LVL	R/W		Digital DAC output clipping control
			0	**disable**
			1	enable

Table 25. Register DAC_CLIPPING (address 10h)

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	CLIP_LVL[7:0]	R/W	-	Digital DAC output clipping level value

Table 26. DAC digital offset registers (address 11h to 14h) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
11h	DAC_A_OFFSET_LSB	7 to 0	DAC_A_OFFSET[7:0]	R/W		DAC A digital offset value
					-	least significant 8 bits for DAC A digital offset
12h	DAC_A_OFFSET_MSB	7 to 0	DAC_A_OFFSET[15:8]		-	most significant 8 bits for DAC A digital offset

Table 26. DAC digital offset registers (address 11h to 14h) bit description *…continued*

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
13h	DAC_B_OFFSET_LSB	7 to 0	DAC_B_OFFSET[7:0]	R/W		DAC B digital offset value
					-	least significant 8 bits for DAC B digital offset
14h	DAC_B_OFFSET_MSB	7 to 0	DAC_B_OFFSET[15:8]		-	most significant 8 bits for DAC B digital offset

Table 27. DAC digital offset registers (address 15h to 17h) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
15h	MUTE_CTRL_0			R/W		mute control
		7	HOLD_DATA		**0**	**disables hold feature**
					1	enables hold feature
		6 to 5	CLIP_SEL[1:0]		**00**	**no mute action**
					01	mute on clip_det_a
					10	mute on clip_det_b
					11	mute on clip_det_a or clip_det_b
		4	CLIP_DET_EN		**0**	**disable clipping detection**
					1	enable clipping detection
		3	MUTE_EN		**0**	**disable mute feature**
					1	enable mute feature
		2 to 0	MUTE_RATE[2:0]			controls the rate of the mute feature at 1 GHz (values below are approximate values for 1 GHz)
					000	~8 ns (immediate)
					001	~125 ns
					010	~500 ns
					100	**~1 µs**
					101	~2 µs
					110	~4 µs
					111	~8 µs

Table 27. DAC digital offset registers (address 15h to 17h) bit description *...continued*

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
16h	MUTE_CTRL1	7 to 6	ALARM_CFG[1:0]	R/W	**00**	**hard mute and mute_iq**
					01	hold mute and mute_iq
					10	soft mute and mute_iq
					11	soft mute
		5 to 4	DATA_V_IQ_CFG[1:0]		**00**	**hard mute and mute_iq**
					01	hold mute and mute_iq
					10	soft mute and mute_iq
					11	soft mute
		3 to 2	CLIP_CFG[1:0]		**00**	**hard mute and mute_iq**
					01	hold mute and mute_iq
					10	soft mute and mute_iq
					11	soft mute
		1 to 0	DIRECT_CFG[1:0]		**00**	**hard mute and mute_iq**
					01	hold mute and mute_iq
					10	soft mute and mute_iq
					11	soft mute
17h	MUTE_CTRL2	7	MC_ALARM_CLR	R/W	0	no action
					1	clear mc_alarm flags
		6	IGN_RFTX_EN		**0**	**no action**
					1	ignore rftx_en state
		5	IGN_MDS_BSY		**0**	**no action**
					1	ignore mds_bsy state
		4	IGN_DATA_V_IQ		**0**	**no action**
					1	ignore internal data-enable state
		0	SW_MUTE		**0**	**no action**
					1	mute signal (uses direct_cfg)

Table 28. Register MUTE_AL_EN (address 18h)

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
				enables alarm condition for mute action
7	DATA_IQ_VAL	R/W	**0**	**1 → 0**
			1	0 → 1
6	MDS_BSY	R/W	**0**	**0 → 1**
			1	1 → 0
5	CLIP_DET_A	R/W	**0**	**0 → 1**
			1	1 → 0
4	CLIP_DET_B	R/W	**0**	**0 → 1**
			1	1 → 0
3	TEMP_ALARM	R/W	**0**	**0 → 1**
			1	1 → 0

Table 28. Register MUTE_AL_EN (address 18h) *…continued*

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
2	CA_ERR	R/W	**0**	**0 → 1**
			1	1 → 0
1	MON_DCLK_ERR	R/W	**0**	**0 → 1**
			1	1 → 0
0	CLK_MON	R/W	**0**	**0 → 1**
			1	1 → 0

Table 29. PAGE_ADDRESS register (address 1Fh) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
4 to 0	PAGE[4:0]	R/W	-	page address

10.17.2 Page x01: Dual DAC core

This page specifies the main analog features of the DAC cores.

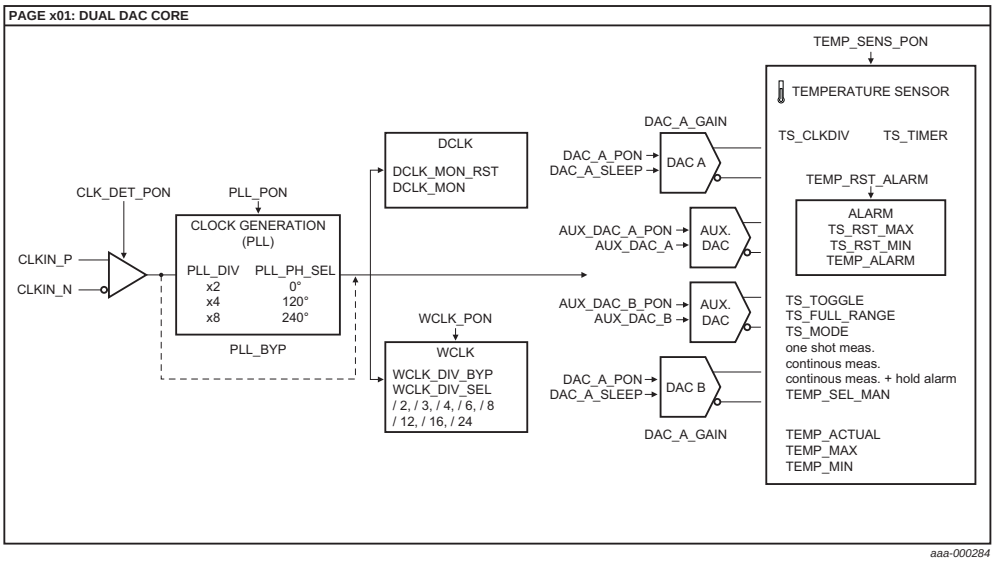


Fig 25. Page x01: Dual DAC core

10.17.2.1 Page x01 allocation map

Table 30 shows an overview of all registers on page x01.

Table 30. Page x01 register allocation map

Address		Register name	R/W	Bit definition								Default	
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
2	02h	PLLCFG	R/W	PLL_BYP	CLK_DET_PON	RESERVED	PLL_DIV[1:0]		PLL_PH_SEL[1:0]		PLL_PON	1010 0001	A1h
4	04h	WCLKGENCFG	R/W	DCLK_MON_RST	DCLK_MON	-	WCLK_PON	WCLK_DIV_BYP	WCLK_DIV_SEL[2:0]			0101 0010	52h
5	05h	TEMPS_CNTRL	R/W	TEMP_SENS_PON	TS_RST_ALARM	TS_FULL_RANGE	TS_TOGGLE	TS_RST_MAX	TS_RST_MIN	TS_MODE[1:0]		0000 0000	00h
6	06h	TEMPS_LEVEL	R/W	-	-	TEMP_SEL_MAN[5:0]						0000 0000	00h
7	07h	TEMPS_CLKDIV	R/W	TS_CLKDIV[7:0]								0000 0000	00h
8	08h	TEMPS_TIMER	R/W	TS_TIMER[7:0]								0000 0000	00h
9	09h	TEMPS_OUT	R	TEMP_SENS_OUT	TEMP_ALARM	TEMP_ACTUAL[5:0]							uuh
10	0Ah	TEMPS_MAX	R	-	-	TEMP_MAX[5:0]							uuh
11	0Bh	TEMPS_MIN	R	-	-	TEMP_MIN[5:0]							uuh
22	16h	DAC_PON_SLEEP	R/W	DAC_A_PON	DAC_B_SLEEP	RESERVED[1:0]		DAC_A_PON	DAC_A_SLEEP	RESERVED[1:0]		1011 1011	BBh
23	17h	DAC_A_GAIN_LSB	R/W	DAC_A_GAIN[7:0]								1101 1000	D8h
24	18h	DAC_A_GAIN_MSB	R/W	DAC_A_GAIN[9:8]		-	-	-	-	-	-	0100 0000	40h
25	19h	DAC_B_GAIN_LSB	R/W	DAC_B_GAIN[7:0]								1101 1011	D8h
26	1Ah	DAC_B_GAIN_MSB	R/W	DAC_B_GAIN[9:8]		-	-	-	-	-	-	0100 0000	40h
27	1Bh	DAC_A_AUX_MSB	R/W	AUX_DAC_A[9:2]								1000 0000	80h

Table 30. Page x01 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default	
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
28	1Ch	DAC_A_AUX_LSB	R/W	AUX_DAC_A_PON	-	-	-	-	-	AUX_DAC_A[1:0]		1000 0000	80h
29	1Dh	DAC_B_AUX_MSB	R/W	AUX_DAC_B[9:2]								1000 0000	80h
30	1Eh	DAC_B_AUX_LSB	R/W	AUX_DAC_B_PON	-	-	-	-	-	AUX_DAC_B[1:0]		1000 0000	80h
31	1Fh	PAGE_ADDRESS	R/W	-	-	-	PAGE[4:0]					0000 0000	00h

10.17.2.2 Page x01 bit definition detailed description

The tables in this section contain detailed descriptions of the page x01 registers.

Table 31. PLLCFG register (address 02h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7	PLL_BYP	R/W	0	DAC clock generated by PLL
			1	DAC clock provided via clock-in (bypass mode)
				PLL_PON must be powered-down when PLL_Bypass is enabled.
6	CLK_DET_PON	R/W	0	PLL input clock detection disabled (power-down)
			1	PLL input clock detection enabled
5	RESERVED	R/W	-	reserved
4 to 3	PLL_DIV[1:0]	R/W	00	DAC at 2 × dclk
			01	DAC at 4 × dclk
			10	DAC at 8 × dclk
			11	undefined
2 to 1	PLL_PH_SEL	R/W	00	DAC clock phase shift = 0°
			01	DAC clock phase shift = 120°
			10	DAC clock phase shift = 240°
			11	DAC clock phase shift = 240°
0	PLL_PON	R/W	0	PLL oscillator output disabled (power-down)
			1	PLL oscillator output enabled.
				PLL_BYP must be disabled when PLL_PON is enabled

Table 32. WCLKGENCFG register (address 04h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7	DCLK_MON_RST	R/W	0	no action
			1	reset dclk_mon_flag
6	DCLK_MON	R	0	dclk_mon OK
			1	dclk_mon failure
4	WCLK_PON	R/W	0	wclk disabled (power-down)
			1	wclk enabled
3	WCLK_DIV_BYP	R/W	0	wclk depends on wclk_div_sel
			1	wclk = DAC clock
2 to 0	WCLK_DIV_SEL[2:0]	R/W	000	wclk = DAC clock / 2
			001	wclk = DAC clock / 3
			010	wclk = DAC clock / 4
			011	wclk = DAC clock / 6
			100	wclk = DAC clock / 12
			110	wclk = DAC clock / 16
			111	wclk = DAC clock / 24

Table 33. TEMPS_CTRL register (address 05h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7	TEMP_SENS_PON	R/W		temperature sensor
			0	disabled (power-down)
			1	enabled
6	TS_RST_ALARM	R/W		reset temperature sensor alarm
			0	no action
			1	reset temp_sensor_alarm flag
5	TS_FULLRANGE	R/W		temperature sensor full range
			0	sweep 22 to 63
			1	sweep 0 to 63
4	TS_TOGGLE	R/W		temperature sensor toggle
			0	wait for 0 → 1 transition
			1	wait for 1 → 0 transition
3	TS_RST_MAX	R/W		temperature sensor, maximum reset
			0	no action
			1	reset temp_max_value
2	TS_RST_MIN	R/W		temperature sensor, minimum reset
			0	no action
			1	reset temp_min_value
1 to 0	TS_MODE[1:0]	R/W		temperature sensor mode
			00	raw mode (direct access to temperature sensor)
			01	one-shot measurement
			10	continuous measurement
			11	continuous measurement (hold temp_alarm_flag)

Table 34. TEMPS_LEVEL register (address 06h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
5 to 0	TEMP_SEL_MAN[5:0]	R/W	-	temperature sensor level selection usage depends on ts_mode: ts_mode = “00”: applied directly to temp_sensor ts_mode = “others”: sets threshold for temp_alarm

Table 35. TEMPS_CLKDIV register (address 07h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	TS_CLKDIV[7:0]	R/W	-	sets clock frequency temp_sensor_cntrl (dclk / ts_clkdiv)

Table 36. TEMPS_TIMER register (address 08h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	TS_TIMER[7:0]	R/W	-	sets number of wait cycles between measurements

Table 37. TEMPS_OUT register (address 09h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7	TEMP_SENS_OUT	R	-	temperature sensor output (for use in raw mode)
6	TEMP_ALARM	R	-	temp_actual > temp_threshold flag
5 to 0	TEMP_ACTUAL[5:0]	R	-	temp_actual (result of last measurement)

Table 38. TEMPS_MAX register (address 0Ah) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
5 to 0	TEMP_MAX[5:0]	R	-	maximum temp_actual found since last ts_rst_max

Table 39. TEMPS_MIN register (address 0Bh) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
5 to 0	TEMP_MIN[5:0]	R	-	minimum temp_actual found since last ts_rst_max

Table 40. DAC_PON_SLEEP register (address 16h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7	DAC_B_PON	R/W		DAC B power
			0	disabled (power-down)
			1	enabled
6	DAC_B_SLEEP	R/W		DAC B sleep mode
			0	normal operation
			1	sleep mode
5 to 4	RESERVED[1:0]	R/W	-	reserved
3	PON_DAC_A	R/W		DAC A power
			0	disabled (power-down)
			1	enabled
2	DAC_A_SLEEP	R/W		DAC A sleep mode
			0	normal operation
			1	sleep mode
1 to 0	RESERVED[1:0]	R/W	-	reserved

Table 41. Analog gain control (address 17h to 1Ah) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
17h	DAC_A_GAIN_LSB	7 to 0	DAC_A_GAIN[7:0]	R/W	-	DAC A analog gain control (LSB)
18h	DAC_A_GAIN_MSB	7 to 6	DAC_A_GAIN[9:8]	R/W	-	DAC A analog gain control (MSB)
19h	DAC_B_GAIN_LSB	7 to 0	DAC_B_GAIN[7:0]	R/W	-	DAC B analog gain control (LSB)
1Ah	DAC_B_GAIN_MSB	7 to 6	DAC_B_GAIN[9:8]	R/W	-	DAC B analog gain control (MSB)

Table 42. Auxiliary DACs registers (address 1Bh to 1Eh) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
1Bh	DAC_A_AUX_MSB	7 to 0	AUX_DAC_A[9:2]	R/W	-	most significant 8 bits for auxiliary DAC A
1Ch	DAC_A_AUX_LSB	7	AUX_DAC_A_PD	R/W		auxiliary DAC A power
					0	**on**
					1	off
		1 to 0	AUX_DAC_A[1:0]		-	least significant 2 bits for auxiliary DAC A
1Dh	DAC_B_AUX_MSB	7 to 0	AUX_DAC_B[9:2]	R/W	-	most significant 8 bits for auxiliary DAC B
1Eh	DAC_B_AUX_LSB	7	AUX_DAC_B_PD	R/W		auxiliary DAC B power
					0	**on**
					1	off
		1 to 0	AUX_DAC_B[1:0]		-	least significant 2 bits for auxiliary DAC B

Table 43. PAGE_ADDRESS register (address 1Fh) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
4 to 0	PAGE[4:0]	R/W	-	SPI page address

10.17.3 Page x02: Multiple devices synchronization and interrupt

This page specifies the configuration of the SYSREF signals (East and West) and how they are used for the multiple devices synchronization (MDS) feature. It also specifies the interrupts.

10.17.3.1 Page x02 allocation map

Table 44 shows an overview of all registers on page x02.

Table 44. Page x02 register allocation map

Address		Register name	R/W	Bit definition								Default[1]	
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
0	00h	MDS_MAIN	R/W	MDS_EQ_CHECK[1:0]		MDS_MAN	MDS_SREF_DIS	MDS_EAST_WEST	MDS_MODE[1:0]		MDS_EN	0000 0000	00h
1	01h	MDS_VS1_CTRL	R/W	DLP_ISSUE_COND[1:0]		IGN_EN_CORR	MDS_DAISY_KEEP_SREF	I_REINIT_MODE[1:0]		-	-	0000 0110	06h
2	02h	MDS_IO_CTRL	R/W	-	-	-	-	MDS_SEL_FE_E	MDS_SEL_RT_E	MDS_SEL_FE_W	MDS_SEL_RT_W	0000 0000	00h
3	03h	MDS_MISC_CTRL0	R/W	MDS_RUN	MDS_NCO	MDS_NCO_PULSE	MDS_EVAL_EN	MDS_PRERUN_EN	MDS_PULSEWIDTH[2:0]			0001 0000	10h
4	04h	MDS_MAN_ADJUST_DLY	R/W	MDS_MAN_ADJUST_DLY[7:0]								1000 0000	80h
5	05h	MDS_AUTO_CYCLES	R/W	MDS_AUTO_CYCLES[7:0]								1000 0000	80h
6	06h	MDS_MISC_CTRL1	R/W	MDS_SR_CKEN	MDS_SR_LOCKOUT	MDS_SR_LOCK	MDS_RELOCK	MDS_LOCK_DLY[3:0]				0000 1111	0Fh
7	07h	MDS_OFFSET_DLY	RW	-	-	-	MDS_OFFSET_DLY[4:0]					0000 0000	00h
8	08h	MDS_WIN_PERIOD_A	R/W	MDS_WIN_PERIOD_A[7:0]								0000 1111	0Fh
9	09h	MDS_WIN_PERIOD_B	R/W	MDS_WIN_PERIOD_B[7:0]								0000 0111	07h
10	0Ah	LMFC_PERIOD	R/W	LMFC_PERIOD[7:0]								0000 1000	08h
11	0Bh	LMFC_PRESET	R/W	LMFC_PRESET[7:0]								0000 0100	04h

Table 44. Page x02 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default[1]	
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
12	0Ch	MDS_CNT_PRESET	R/W	MDS_CNT_PRESET[7:0]								0000 0010	02h
13	0Dh	SYNC_LMFC_PE	R/W	SYNC_LMFC_PE[7:0]								0000 0100	04
14	0Eh	MDS_SYNC_CTRL	R/W	-	-	-	MDS_ SYNC_ INIT	-	SYNC_FINE_DLY[2:0]			0000 0100	04h
16	10h	MDS_DAISY_CYCLES	R/W	MDS_DAISY_CYCLES[7:0]								0000 0100	04h
17	11h	MDS_WAIT_CYCLES	R/W	MDS_WAIT_CYCLES								0000 0100	04h
19	13h	ERR_RPT_CTRL	R/W	-	-	-	-	-	ERR_RPT_CTRL[2:0]			0000 0000	00h
20	14h	ERR_RPT_POS	R/W	ERR_RPT_POS[7:0]									
21	15h	MDS_ADJ_DLY	RW	MDS_ADJ_DLY[7:0]								uuuu uuuu	uuh
22	16h	MDS_STATUS0	R	EARLY	LATE	EQUAL	MDS_EQ	EARLY_ ERR	LATE_ ERR	EQUAL_ FOUND	MDS_ ACTIVE	uuuu uuuu	uuh
23	17h	MDS_STATUS1	R	RPT_ FLAG_ ERR	I_BSY	ADD_ERR	PH_EN[1:0]		MDS_ PRERUN	MDS_ LOCKOUT	MDS_ LOCK	uuuu uuuu	uuh
24	18h	INTR_CTRL	R/W	-	-	-	-	INTR_CLR	INTR_MON_DCLK_RANGE[2:0]			0000 0000	00h
25	19h	INTR_EN_0	R/W	INTR_EN[7:0]								0000 0000	00h
26	1Ah	INTR_EN_1	R/W	-	INTR_EN[14:8]							0000 0011	03h
27	1Bh	INTR_FLAGS_0	R/W	INTR_DLP	$\overline{\text{MDS\_BSY}}$	MDS_ BSY	TEMP_ ALARM	CLIP_DET _OR	CA_ ERROR	CLK_MON	MON_ DCLK_ ERR	uuuu uuuu	uuh

Table 44. Page x02 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default[1]	
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
28	1Ch	INTR_FLAGS_1	R/W	-	RPT_FLAG_ERR	MC_ALARM	MAQ_RDY_B	MAQ_RDY_A	AUTO_DL_RDY	AUTO_CAL_RDY	FLAG_DL_ERR	uuuu uuuu	uuh
31	15h	PAGE_ADDRESS	R/W	-	-	-			PAGE[4:0]			0000 0000	00h

[1] u = undefined at power-up or after reset.

10.17.3.2 Page x02 bit definition detailed description

The tables in this section contain detailed descriptions of the page x02 registers.

Table 45. MDS_MAIN register (address 00h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	MDS_EQ_CHECK[1:0]	R/W		lock mode
			00	**lock when (early = 1 and late = 1)**
			01	lock when (early = 1, late = 1 and equal = 1)
			10	lock when equal = 1
			11	force lock (equal-check = 1)
5	MDS_MAN	R/W		control adjustment delays
			0	**auto-control adjustment delays**
			1	manual control adjustment delays
4	MDS_SREF_DIS	R/W		sref generation
			0	**disabled**
			1	enabled
3	MDS_EAST_WEST	R/W		MDS input/output
			0	west used as MDS input
			1	east used as MDS input
2 to 1	MDS_MODE[1:0]	R/W		MDS mode
			00	mds_vs0 all-slave mode
			01	mds_vs0 master mode
			10	mds_vs1 without daisy-chain control
			11	mds_vs1 with daisy-chain control
0	MDS_EN	R/W		MDS function control
			0	**disabled**
			1	enabled

Table 46. MDS_VS1_CTRL register (address 01h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	DLP_ISSUE_COND[1:0]	R/W		digital lane processing issue condition that generates an error in the MDS module
			00	dlp_issue ≤ ($\overline{\text{dlp\_lock}}$) OR ($\overline{\text{dlp\_sync}}$)
			01	dlp_issue ≤ ($\overline{\text{dlp\_lock}}$) AND ($\overline{\text{dlp\_sync}}$)
			10	dlp_issue ≤ ($\overline{\text{dlp\_lock}}$)
			11	dlp_issue ≤ ($\overline{\text{dlp\_sync}}$)
5	IGN_EN_CORR	R/W		DLP/CDI-latency uncertainty correction
			0	compensate for DLP/CDI-latency uncertainty
			1	no correction for DLP/CDI-latency uncertainty

Table 46. MDS_VS1_CTRL register (address 01h) bit description *…continued*

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
4	MDS_DAISY_KEEP_SREF	R/W		controls the SREF signal generation in daisy chain mode, for easy resynchronization
			0	daisy control timer switches sref off
			1	sref used for daisy chain remains active
3 to 2	I_REINIT_MODE[1:0]	R/W		reinitialization mode
			00	assert synchronization request
			01	assert synchronization request and reset DLP
			10	assert synchronization request and reset MDS controller
			11	no action (ignore dlp_issue)

Table 47. MDS_IO_CTRL register (address 02h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
3	MDS_SEL_FE_E	R/W		MDS east falling edge/rising edge operation
			0	falling edge
			1	rising edge
2	MDS_SEL_RT_E	R/W		MDS east internal resistor termination activation
			0	inactive
			1	active
1	MDS_SEL_FE_W	R/W		MDS west falling edge/rising edge operation
			0	falling edge
			1	rising edge
0	MDS_SEL_RT_W	R/W		MDS west internal resistor termination activation
			0	inactive
			1	active

Table 48. MDS_MISC_CTRL0 register (address 03h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7	MDS_RUN	R/W		starts the MDS module
			0	no action
			1	(0 → 1) transition restarts evaluation counter
6	MDS_NCO	R/W		NCO synchronization
			0	disabled
			1	enabled
5	MDS_NCO_PULSE	R/W		NCO tuning manual control
			0	disabled
			1	enabled
4	MDS_EVAL_EN	R/W		MDS evaluation
			0	disabled
			1	**enabled**

Table 48. MDS_MISC_CTRL0 register (address 03h) bit description *…continued*

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
3	MDS_PRERUN_EN	R/W		automatic MDS start-up
			0	**no mds_win/mds_ref generation in advance**
			1	mds_win/mds_ref run-in before mds_evaluation
2 to 0	MDS_PULSEWIDTH[2:0]	R/W		width of MDS (in output clock periods)
			000	**1 DAC clock period**
			001	2 DAC clock periods
			010 to 111	(mds_pulsewidth − 1) × 4 DAC clock periods

Table 49. MDS_MAN_ADJUST_DLY register (address 04h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	MDS_MAN_ADJUST_DLY[6:0]	R/W		adjustment delay value
			0	if MDS_MAN = 0 then initial value adjustment delay
			1	if MDS_MAN = 1 then controls adjustment delay

Table 50. MDS_AUTO_CYCLES register (address 05h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	MDS_AUTO_CYCLES[7:0]	R/W	-	number of evaluation cycles applied for MDS.

Table 51. MDS_MISC_CTRL1 register (address 06h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7	MDS_SR_CKEN	R/W	-	lock mode
			0	**free-running MDS_SR_CKEN**
			1	MDS_SR_CKEN forced low
6	MDS_SR_LOCKOUT	R/W		lockout detector soft reset
			0	**MDS_SR_LOCKOUT in use**
			1	MDS_SR_LOCKOUT forced low
5	MDS_SR_LOCK	R/W		lock detector soft reset
			0	**MDS_SR_LOCK in use**
			1	MDS_SR_LOCK forced low
4	MDS_RELOCK	R/W		relock mode
			0	**no action**
			1	relock when lockout occurs
3 to 0	MDS_LOCK_DLY[3:0]	R/W	-	number of succeeding 'equal' detections until lock

Table 52. MDS_OFFSET_DLY register (address 07h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
4 to 0	MDS_OFFSET_DLY[6:0]	R/W	-	delay offset for dataflow (two's complement [−16 to 15]

Table 53. MDS window registers (address 08h to 09h) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
08h	MDS_WIN_PERIOD_A	7 to 0	MDS_WIN_PERIOD_A[7:0]	R/W	-	determines MDS window LOW time
09h	MDS_WIN_PERIOD_B	7 to 0	MDS_WIN_PERIOD_B[7:0]	R/W	-	determines MDS window HIGH time

Table 54. LMFC_PERIOD register (address 0Ah) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	LMFC_PERIOD[7:0]	R/W	-	determines the LMFC period

Table 55. LMFC_PRESET register (address 0Bh) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	LMFC_PRESET[7:0]	R/W	-	delays the LMFC period as related to the internal sref signal

Table 56. MDS_CNT_PRESET register (address 0Ch) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	MDS_CNT_PRESET[7:0]	R/W	-	determines the sref position as related to the sysref signal

Table 57. SYNC_LMFC_PE register (address 0Dh) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	SYNC_LMFC_PE[7:0]	R/W	-	determines the pos_edge SYNCB position pos_edge as related to LMFC

Table 58. MDS_SYNC_CTRL register (address 0Eh) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
4	MDS_SYNC_INIT	R/W		MDS synchronization initialization
			0	initial state SYNCB = ‘0’.
			1	initial state SYNCB = ‘1’.
2 to 0	SYNC_FINE_DLY[2:0]	R/W	-	fine-tuning SYNCB position (sync_rq × (dacclk – accuracy))

Table 59. MDS_DAISY_CYCLES register (address 10h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	MDS_DAISY_CYCLES[7:0]	R/W	-	number of digital clock periods required to synchronize daisy partner

Table 60. MDS_WAIT_CYCLES register (address 11h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	MDS_WAIT_CYCLES[7:0]	R/W	-	number of daisy cycles required before releasing DLP

Table 61. RPT_CTRL_ERR register (address 13h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
2 to 0	RPT_CTRL_ERR[2:0]	R/W		error reporting pulse width
			00x	no error reporting pulse width
			010	err_rpt_pulse_width = 2 DAC clock periods
			011	err_rpt_pulse_width = 4 DAC clock periods
			100	err_rpt_pulse_width = 8 DAC clock periods
			101	err_rpt_pulse_width = 16 DAC clock periods
			110	err_rpt_pulse_width = 32 DAC clock periods
			111	err_rpt_pulse_width = 64 DAC clock periods

Table 62. RPT_POS_ERR register (address 14h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
6 to 0	RPT_POS_ERR[7:0]	R/W	-	determines err_rpt position as related to LMFC

Table 63. MDS_ADJ_DLY register (address 15h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
6 to 0	MDS_ADJ_DLY[6:0]	R	-	actual value adjustment delay

Table 64. MDS_STATUS registers (address 16h to 17h) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
16h	MDS_STATUS0	7	EARLY	R		early signal (sampled) from early-to-late detector
					0	false
					1	true
		6	LATE	R		late signal (sampled) from early-to-late detector
					0	false
					1	true
		5	EQUAL	R		equal signal (sampled) from early-to-late detector
					0	false
					1	true
		4	MDS_LOCK	R		result equal-check
					0	false
					1	true
		3	EARLY_ERR	R		adjustment delay maximum value stops the search
					0	false
					1	true
		2	LATE_ERR	R		adjustment delay minimum value stops the search
					0	false
					1	true
		1	EQUAL_FOUND	R		evaluation logic has detected equal condition
					0	false
					1	true
		0	MDS_ACTIVE			evaluation logic active
					0	false
					1	true

Table 64. MDS_STATUS registers (address 16h to 17h) bit description *…continued*

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
17h	MDS_STATUS1	5	ADD_ERR	R		adjustment delay error detection
					0	OK
					1	delay offset cannot be applied within available range
		4 to 3	MDS_EN_PHASE[1:0]	R		MDS enable phase
					00	enable phase = 0
					01	enable phase = 1 (only for ^2)
					10	enable phase = 2 (only for ^2 CDI mode and ^4 CDI mode)
					11	enable phase = 3 (only for ^2)
		2	MDS_PRERUN	R		MDS-PRERUN phase active flag
					0	false
					1	true
		1	MDS_LOCKOUT	R		MDS_LOCKOUT detected flag
					0	false
					1	true
		0	MDS_LOCK	R		MDS_LOCK flag
					0	false
					1	true

Table 65. INTR_CTRL register (address 18h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
3	INTR_CLR	R/W		i_intr and i_flags clearance
			0	disabled
			1	enabled
2 to 0	INTR_MON_DCLK_RANGE[2:0]	R/W		interrupt condition as related to the DCLK monitoring
			000	mon_dclk_flag when mon_dclk drifts to (1 | 9)
			001	mon_dclk_flag when mon_dclk drifts to (2 | 8)
			010	mon_dclk_flag when mon_dclk drifts to (3 | 7)
			011	mon_dclk_flag when mon_dclk drifts to (4 | 6)
			100	mon_dclk_flag when mon_dclk drifts to (5)
			others	mon_dclk_flag disabled

Table 66. INTR_EN registers (address 19h to 1Ah) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
19h	INTR_EN_0	7 to 0	INTR_EN[7:0]	R/W	-	enables usage of intr_src[7:0] for intr_flags[7:0]
1Ah	INTR_EN_1	6 to 0	INTR_EN[14:8]	R/W	-	enables usage of intr_src[14:8] for intr_flags[14:8]

Table 67. INTR_FLAGS registers (address 19h to 1Ah) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
1Bh	INTR_FLAGS_0	7	INTR_DLP	R	-	intr_dlp active
		6	$\overline{\text{MDS\_BSY}}$		-	indicates transition 1 → 0 on mds_busy
		5	MDS_BSY		-	indicates transition 0 → 1 on mds_busy
		4	TEMP_ALARM		-	indicates transition 0 → 1 on temp_alarm
		3	CLIP_DET_OR		-	indicates transition 0 → 1 on clip_detect (a or b)
		2	CA_ERR		-	indicates transition 0 → 1 on clock_align_monitor
		1	CLK_MON		-	indicates transition 0 → 1 on clkmon (div8)
		0	MON_DCLK_ERR		-	indicates transition 0 → 1 on mon_dclk_error_flags
1Ch	INTR_FLAGS_1	6	RPT_FLAG_ERR	R	-	indicates transition 0 → 1 on err_rpt_flag
		5	MC_ALARM		-	indicates alarm event detected by mute_cntrl
		4	MAQ_RDY_B		-	indicates that acquisition_module B is ready
		3	MAQ_RDY_A		-	indicates that acquisition_module#A is ready
		2	AUTO_DL_RDY		-	indicates that auto_download_mtp is done
		1	AUTO_CAL_RDY		-	indicates that auto_calibration is done
		0	FLAG_DL_ERR		-	indicates transition 0 → 1 on err_flag_download_mtp

Table 68. PAGE_ADDRESS register (address 1Fh) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
4 to 0	PAGE[4:0]	R/W	-	SPI page address

10.17.4 Page x03: RX Digital Lane Processing (DLP)

This page specifies the configuration of the digital lane processing.

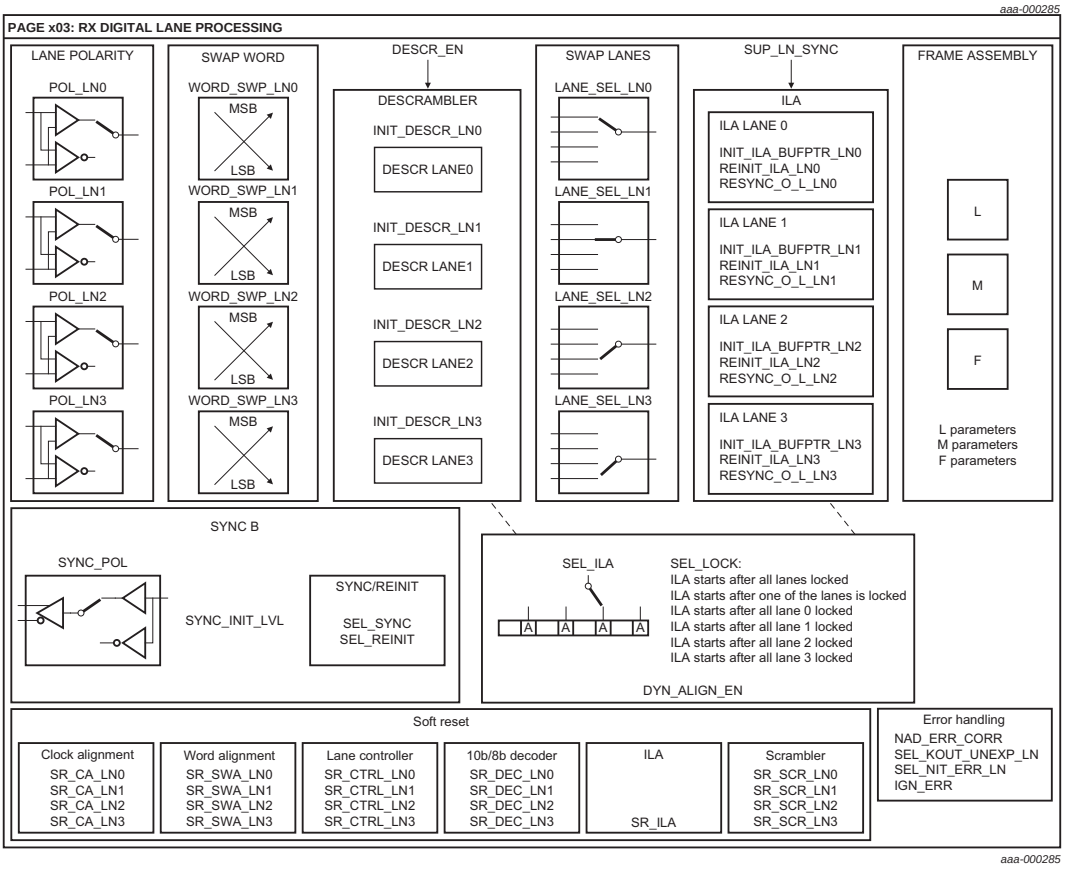


Fig 26. Page x03: RX digital lane processing

10.17.4.1 Page x03 allocation map

Table 69 shows an overview of all registers on page x03.

Table 69. Page x03 register allocation map

Address		Register name	R/W	Bit definition								Default	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
0	00h	SR_DLP_0	R/W	SR_SWA_LN3	SR_SWA_LN2	SR_SWA_LN1	SR_SWA_LN0	SR_CA_LN3	SR_CA_LN2	SR_CA_LN1	SR_CA_LN0	0000 0000	00h
1	01h	SR_DLP_1	R/W	SR_CTRL_LN3	SR_CTRL_LN2	SR_CTRL_LN1	SR_CTRL_LN0	SR_DEC_LN3	SR_DEC_LN2	SR_DEC_LN1	SR_DEC_LN0	0000 0000	00h
2	02h	FORCE_LOCK	R/W	FORCE_LOCK_LN3	FORCE_LOCK_LN2	FORCE_LOCK_LN1	FORCE_LOCK_LN0	-	-	FRAME_ALIGN_EN	SR_ILA	0000 0000	00h
3	03h	MAN_LOCK_LN_1_0	R/W	MAN_LOCK_LN1[3:0]				MAN_LOCK_LN0[3:0]				0000 0000	00h
4	04h	MAN_LOCK_LN_3_2	R/W	MAN_LOCK_LN3[3:0]				MAN_LOCK_LN2[3:0]				0000 0000	00h
5	05h	CA_CTRL	R/W	WORD_SWP_LN3	WORD_SWP_LN2	WORD_SWP_LN1	WORD_SWP_LN0	SEL_RF_F10_LN3	SEL_RF_F10_LN2	SEL_RF_F10_LN1	SEL_RF_F10_LN0	0000 0000	00h
6	06h	SCR-CTRL	R/W	MAN_SCR_LN3	MAN_SCR_LN2	MAN_SCR_LN1	MAN_SCR_LN0	FORCE_SCR_LN3	FORCE_SCR_LN2	FORCE_SCR_LN1	FORCE_SCR_LN0	0000 0000	00h
7	07h	ILA_CTRL	R/W	-	SEL_ILA[1:0]		SEL_LOCK[2:0]			SUP_LN_SYNC	DESCR_EN	0000 0011	03h
8	08h	FORCE_ALIGN	R/W	-	-	MSB_MAN_LOCK_LN[3:0]				DYN_ALIGN_EN	FORCE_ALIGN	0000 0000	00h
9	09h	MAN_ALIGN_LN_1_0	R/W	MAN_ALIGN_LN1[3:0]				MAN_ALIGN_LN0[3:0]				0000 0000	00h
10	0Ah	MAN_ALIGN_LN_3_2	R/W	MAN_ALIGN_LN3[3:0]				MAN_ALIGN_LN2[3:0]				0000 0000	00h
11	0Bh	FA_ERR_HANDLING	R/W	SEL_KOUT_UNEXP_LN32[1:0]		SEL_KOUT_UNEXP_LN10[1:0]		SEL_NIT_ERR_LN32[1:0]		SEL_NIT_ERR_LN10[1:0]		0000 0000	00h
12	0Ch	SYNCOUT_MODE	R/W	SEL_REINIT[2:0]			SYNC_POL	SYNC_INIT_LVL	SEL_SYNC[3:0]			0000 0000	00h
13	0Dh	LANE_POLARITY	R/W	-	-	-	-	POL_LN3	POL_LN2	POL_LN1	POL_LN0	0000 0000	00h
14	0Eh	LANE_SELECT	R/W	LANE_SEL_LN3[1:0]		LANE_SEL_LN2[1:0]		LANE_SEL_LN1[1:0]		LANE_SEL_LN0[1:0]		1110 0100	E4h

Table 69. Page x03 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
16	10h	SOFT_RESET_ SCRAMBLER	R/W	-	-	-	-	SR_SCR_ LN3	SR_SCR_ LN2	SR_SCR_ LN1	SR_SCR_ LN0	0000 0000	00h
17	11h	INIT_SCR_S15T8 _LN0	R/W	INIT_DESCR_LN0[15:8]								0000 0000	00h
18	12h	INIT_SCR_ S7T1_LN0	R/W	-	INIT_DESCR_LN0[[6:0]							0000 0000	00h
19	13h	INIT_SCR_ S15T8_LN1	R/W	INIT_DESCR_LN1[15:8]								0000 0000	00h
20	14h	INIT_SCR_ S7T1_LN1	R/W	-	INIT_DESCR_LN1[[6:0]							0000 0000	00h
21	15h	INIT_SCR_ S15T8_LN2	R/W	INIT_DESCR_LN2[15:8]								0000 0000	00h
22	16h	INIT_SCR_ S7T1_LN2	R/W	-	INIT_DESCR_LN2[[6:0]							0000 0000	00h
23	17h	INIT_SCR_ S15T8_LN3	R/W	INIT_DESCR_LN3[15:8]								0000 0000	00h
24	18h	INIT_SCR_ S7T1_LN3	R/W	-	INIT_DESCR_LN3[[6:0]							0000 0000	00h
25	19h	INIT_ILA_ BUFPTR_LN_1_0	R/W	INIT_ILA_BUFPTR_LN1[3:0]				INIT_ILA_BUFPTR_LN0[3:0]				1000 1000	88h
26	1Ah	INIT_ILA_ BUFPTR_LN_3_2	R/W	INIT_ILA_BUFPTR_LN3[3:0]				INIT_ILA_BUFPTR_LN2[3:0]				1000 1000	88h
27	1Bh	ERROR_ HANDLING	R/W	-	NAD_ERR_ CORR	-	-	-	-	-	IGN_ERR	0000 0000	00h
28	1Ch	REINIT_CTRL	R/W	REINIT_ ILA_LN3	REINIT_ILA_ LN2	REINIT_ILA_ LN1	REINIT_ILA_ LN0	RESYNC_ O_L_LN3	RESYNC_ O_L_LN2	RESYNC_ O_L_LN1	RESYNC_ O_L_LN0	0000 0000	00h
29	1Dh	MISC_CTRL	R/W	DLP_ STROBE	-	-	-	-	-	RESERVED[1:0]		0000 0000	00h
30	1Eh	LMF_CTRL	R/W	L[2:0]			M[1:0]		F[2:0]			1001 0010	92h
31	1Fh	PAGE_ADDRESS	R/W	-	-	-	PAGE[4:0]					0000 0000	00h

10.17.4.2 Page x03 bit definition detailed description

The tables in this section contain detailed descriptions of the page x03 registers.

Table 70. Soft reset DLP registers (address 00h to 01h) bit description

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
00h	SR_DLP_0	7	SR_SWA_LN3	R/W	0	soft reset sync_word_alignment lane 3
		6	SR_SWA_LN2		0	soft reset sync_word_alignment lane 2
		5	SR_SWA_LN1		0	soft reset sync_word_alignment lane 1
		4	SR_SWA_LN0		0	soft reset sync_word_alignment lane 0
		3	SR_CA_LN3		0	soft reset clock_alignment lane 3
		2	SR_CA_LN2		0	soft reset clock_alignment lane 2
		1	SR_CA_LN1		0	soft reset clock_alignment lane 1
		0	SR_CA_LN0		0	soft reset clock_alignment lane 0
01h	SR_DLP_1	7	SR_CTRL_LN3	R/W	0	soft reset controller lane 3
		6	SR_CTRL_LN2		0	soft reset controller lane 2
		5	SR_CTRL_LN1		0	soft reset controller lane 1
		4	SR_CTRL_LN0		0	soft reset controller lane 0
		3	SR_DEC_LN3		0	soft reset decoder_10b8b lane 3
		2	SR_DEC_LN2		0	soft reset decoder_10b8b lane 2
		1	SR_DEC_LN1		0	soft reset decoder_10b8b lane 1
		0	SR_DEC_LN0		0	soft reset decoder_10b8b lane 0

Table 71. FORCE_LOCK register (address 02h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	FORCE_LOCK_LN3	R/W		lane 3 lock mode
			0	**automatic lock sync_word_alignment lane 3**
			1	manual lock sync_word_alignment lane 3
6	FORCE_LOCK_LN2	R/W		lane 2 lock mode
			0	**automatic lock sync_word_alignment lane 2**
			1	manual lock sync_word_alignment lane 2
5	FORCE_LOCK_LN1	R/W		lane 1 lock mode
			0	**automatic lock sync_word_alignment lane 1**
			1	manual lock sync_word_alignment lane 1
4	FORCE_LOCK_LN0	R/W		lane 0 lock mode
			0	**automatic lock sync_word_alignment lane 0**
			1	manual lock sync_word_alignment lane 0
1	FRAME_ALIGN_EN	R/W		frame alignment
			0	**no action**
			1	enable frame alignment
0	SR_ILA	R/W		soft reset inter-lane alignment
			0	**no action**
			1	reset

Table 72. Manual lock registers (address 03h to 04h) bit description

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
03h	MAN_LOCK_LN_1_0	7 to 4	MAN_LOCK_LN1[3:0]	R/W	0h	manual lock setting synchronization word alignment lane 1
		3 to 0	MAN_LOCK_LN0[3:0]		0h	manual lock setting synchronization word alignment lane 0
04h	MAN_LOCK_LN_3_2	7 to 4	MAN_LOCK_LN3[3:0]	R/W	0h	manual lock setting synchronization word alignment lane 3
		3 to 0	MAN_LOCK_LN2[3:0]		0h	manual lock setting synchronization word alignment lane 2

Table 73. CA_CTRL register (address 05h) bit description

Bit	Symbol	Access	Value	Description
7	WORD_SWP_LN3	R/W		lane 3 bit swapping
			0	**dout_ca_ln3[7:0] = din_ca_ln3[7:0]**
			1	dout_ca_ln3[7:0] = din_ca_ln3[0:7]
6	WORD_SWP_LN2	R/W		lane 2 bit swapping
			0	**dout_ca_ln2[7:0] = din_ca_ln2[7:0]**
			1	dout_ca_ln2[7:0] = din_ca_ln2[0:7]
5	WORD_SWP_LN1	R/W		lane 1 bit swapping
			0	**dout_ca_ln1[7:0] = din_ca_ln1[7:0]**
			1	dout_ca_ln1[7:0] = din_ca_ln1[0:7]
4	WORD_SWP_LN0	R/W		lane 0 bit swapping
			0	**dout_ca_ln0[7:0] = din_ca_ln0[7:0]**
			1	dout_ca_ln0[7:0] = din_ca_ln0[0:7]
3	SEL_RF_F10_LN3	R/W		lane 3 sampling mode
			0	**din_ca_ln3 sampled at falling edge f10_ln3**
			1	din_ca_ln3 sampled at rising edge f10_ln3
2	SEL_RF_F10_LN2	R/W		lane 2 sampling mode
			0	**din_ca_ln2 sampled at falling edge f10_ln2**
			1	din_ca_ln2 sampled at rising edge f10_ln2
1	SEL_RF_F10_LN1	R/W		lane 1 sampling mode
			0	**din_ca_ln1 sampled at falling edge f10_ln1**
			1	din_ca_ln1 sampled at rising edge f10_ln1
0	SEL_RF_F10_LN0	R/W		lane 0 sampling mode
			0	**din_ca_ln0 sampled at falling edge f10_ln0**
			1	din_ca_ln0 sampled at rising edge f10_ln0

Table 74. SCR_CNTRL register (address 06h) bit description

Bit	Symbol	Access	Value	Description
7	MAN_SCR_LN3	R/W		lane 3 manual scrambling
			0	**scrambling lane 3 off (when force_scr_ln3 = 1)**
			1	scrambling lane 3 on (when force_scr_ln3 = 1)
6	MAN_SCR_LN2	R/W		lane 2 manual scrambling
			0	**scrambling lane 2 off (when force_scr_ln2 = 1)**
			1	scrambling lane 2 on (when force_scr_ln2 = 1)
5	MAN_SCR_LN1	R/W		lane 1 manual scrambling
			0	**scrambling lane 1 off (when force_scr_ln1 = 1)**
			1	scrambling lane 1 on (when force_scr_ln1 = 1)
4	MAN_SCR_LN0	R/W		lane 0 manual scrambling
			0	**scrambling lane 0 off (when force_scr_ln0 = 1)**
			1	scrambling lane 0 on (when force_scr_ln0 = 1)
3	FORCE_SCR_LN3	R/W		lane 3 scrambling mode
			0	**scrambling lane 3 depends on lock_ln3 and en_scr**
			1	scrambling lane 3 depends on man_scr_ln3
2	FORCE_SCR_LN2	R/W		lane 2 scrambling mode
			0	**scrambling lane 2 depends on lock_ln2 and en_scr**
			1	scrambling lane 2 depends on man_scr_ln2
1	FORCE_SCR_LN1	R/W		lane 1 scrambling mode
			0	**scrambling lane 1 depends on lock_ln1 and en_scr**
			1	scrambling lane 1 depends on man_scr_ln1
0	FORCE_SCR_LN0	R/W		lane 0 scrambling mode
			0	**scrambling lane 0 depends on lock_ln0 and en_scr**
			1	scrambling lane 0 depends on man_scr_ln0

Table 75. ILA_CTRL register (address 07h) bit description

Bit	Symbol	Access	Value	Description
6 to 5	SEL_ILA[1:0]	R/W		inter-lane alignment trigger mode
			00	**inter-lane alignment is done after receiving 1 /A/-symbol**
			01	inter-lane alignment is done after receiving 2 /A/-symbols
			10	inter-lane alignment is done after receiving 3 /A/-symbols
			11	inter-lane alignment is done after receiving 4 /A/-symbols
4 to 2	SEL_LOCK[2:0]	R/W		inter-lane alignment start mode
			000	**inter-lane alignment can only start if all (4 or 2) lanes are locked**
			001	inter-lane alignment can start if one of the (4 or 2) lanes are locked
			010	inter-lane alignment can start if lane 0 is locked
			011	inter-lane alignment can start if lane 1 is locked
			100	inter-lane alignment can start if lane 2 is locked
			101	inter-lane alignment can start if lane 3 is locked
1	SUP_LN_SYNC	R/W		inter-lane alignment enable
			0	inter-lane alignment synchronization disabled
			1	**inter-lane alignment synchronization enabled**
0	DESCR_EN	R/W		data descrambling
			0	disabled
			1	**enabled**

Table 76. FORCE_ALIGN register (address 08h) bit description

Bit	Symbol	Access	Value	Description
5 to 2	MSB_MAN_LOCK_LN[3:0]	R/W	-	most significant 4 bits of man_lock_ln
1	DYN_ALIGN_EN	R/W		dynamic realignment mode
			0	**no dynamic realignment**
			1	dynamic realignment (and monitoring) enabled
0	FORCE_ALIGN	R/W		lane alignment mode
			0	**automatic lane alignment based on /A/ symbols**
			1	manual lane alignment based on man_align_lnx

Table 77. Manual alignment registers (address 09h to 0Ah) bit description

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
09h	MAN_ALIGN_LN_1_0	7 to 4	MAN_ALIGN_LN1[3:0]	R/W	0h	indicates alignment data-delay for lane 1 [1..15]
		3 to 0	MAN_ALIGN_LN0[3:0]		0h	indicates alignment data-delay for lane 0 [1..15]
0Ah	MAN_ALIGN_LN_3_2	7 to 4	MAN_ALIGN_LN3[3:0]	R/W	0h	indicates alignment data-delay for lane 3 [1..15]
		3 to 0	MAN_ALIGN_LN2[3:0]		0h	indicates alignment data-delay for lane 2 [1..15]

Table 78. FA_ERR_HANDLING register (address 0Bh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	SEL_KOUT_ UNEXP_LN32[1:0]	R/W		lane 3/lane 2 unexpected /K/ error handling
			00	**unexpected /K/ in lane 2 or lane 3 error_handling**
			01	unexpected /K/ in lane 2 and lane 3 error_handling
			10	unexpected /K/ in lane 2 error_handling
			11	unexpected /K/ in lane 3 error_handling
5 to 4	SEL_KOUT_ UNEXP_LN10[1:0]	R/W		lane 1/lane 0 unexpected /K/ error handling
			00	**unexpected /K/ in lane 0 or lane 1 error_handling**
			01	unexpected /K/ in lane 0 and lane 1 error_handling
			10	unexpected /K/ in lane 0 error_handling
			11	unexpected /K/ in lane 1 error_handling
3 to 2	SEL_NIT_ERR_ LN32[1:0]	R/W		lane 3/lane 2 nit-error handling
			00	**nit-errors in lane 2 or lane 3 error_handling**
			01	not-in-table errors lane 2 and lane 3 error_handling
			10	not-in-table errors in lane 2 error_handling
			11	not-in-table errors in lane 3 error_handling
1 to 0	SEL_NIT_ERR_ LN10[1:0]	R/W		lane 1/lane 0 nit-error handling
			00	**nit-errors in lane 0 or lane 1 error_handling**
			01	not-in-table errors lane 0 and lane 1 error_handling
			10	not-in-table errors in lane 0 error_handling
			11	not-in-table errors in lane 1 error_handling

Table 79. SYNCOUT_MODE register (address 0Ch) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	SEL_RE_INIT[2:0]	R/W		reinitialization mode
			000	**reinitialization request when 1 of the lane resets is active**
			001	reinitialization request when rst_ln0 or rst_ln1 is active
			010	reinitialization request when rst_ln2 or rst_ln3 is active
			011	reinitialization request when rst_ln0 is active
			100	reinitialization request when rst_ln1 is active
			101	reinitialization request when rst_ln2 is active
			110	reinitialization request when rst_ln3 is active
			111	reinitialization request remains '0'
4	SYNC_POL	R/W		synchronization polarity
			0	**sync_out is active when LOW**
			1	sync_out is active when HIGH
3	SYNC_INIT_LVL	R/W		synchronization initialization level
			0	synchronization starts with ‘0’
			1	synchronization starts with ‘1’
2 to 0	SEL_SYNC[2:0]	R/W		synchronization mode
			0000	**synchronization when one of the four lane_syncs is active**
			0001	synchronization when all four lane_syncs are active
			0010	synchronization when sync_ln0 or sync_ln1 is active
			0011	synchronization when both sync_ln0 and sync_ln1 are active
			0100	synchronization when sync_ln2 or sync_ln3 is active
			0101	synchronization when both sync_ln2 and sync_ln3 are active
			0110	synchronization when sync_ln0 is active
			0111	synchronization when sync_ln1 is active
			1000	synchronization when sync_ln2 is active
			1001	synchronization when sync_ln3 is active
			1010	synchronization remains fixed '1'
			other	synchronization remains fixed '0'

Table 80. LANE_POLARITY register (address 0Dh) bit description

Bit	Symbol	Access	Value	Description
3	POL_LN3	R/W		lane 3 data polarity
			0	**no action**
			1	invert all data bits of lane 3

Table 80. LANE_POLARITY register (address 0Dh) bit description *...continued*

Bit	Symbol	Access	Value	Description
2	POL_LN2	R/W		lane 2 data polarity
			0	**no action**
			1	invert all data bits of lane 2
1	POL_LN1	R/W		lane 1 data polarity
			0	**no action**
			1	invert all data bits of lane 1]
0	POL_LN0	R/W		lane 0 data polarity
			0	**no action**
			1	invert all data bits of lane 0

Table 81. LANE_SELECT register (address 0Eh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	LANE_SEL_LN3[1:0]	R/W		lane 3 data mapping
				lane swapping occurs at the end of the DLP. All the registers linked to lane 0/lane 1/lane 2/lane 3 refer to the physical lanes, not the logical ones after swapping.
			00	physical lane 3 is mapped to internal lane 0
			01	physical lane 3 is mapped to internal lane 1
			10	physical lane 3 is mapped to internal lane 2
			11	**physical lane 3 is mapped to internal lane 3**
5 to 4	LANE_SEL_LN2[1:0]	R/W		lane 2 data mapping
			00	physical lane 2 is mapped to internal lane 0
			01	physical lane 2 is mapped to internal lane 1
			10	**physical lane 2 is mapped to internal lane 2**
			11	physical lane 2 is mapped to internal lane 3
3 to 2	LANE_SEL_LN1[1:0]	R/W		lane 1 data mapping
			00	physical lane 1 is mapped to internal lane 0
			01	**physical lane 1 is mapped to internal lane 1**
			10	physical lane 1 is mapped to internal lane 2
			11	physical lane 1 is mapped to internal lane 3
1 to 0	LANE_SEL_LN0[1:0]	R/W		lane 0 data mapping
			00	**physical lane 0 is mapped to internal lane 0**
			01	physical lane 0 is mapped to internal lane 1
			10	physical lane 0 is mapped to internal lane 2
			11	physical lane 0 is mapped to internal lane 3

Table 82. SOFT_RESET_SCRAMBLER register (address 10h) bit description

Bit	Symbol	Access	Value	Description
3	SR_SCR_LN3	R/W		lane 3 scrambler reset
			0	**no action**
			1	soft_reset scrambler of lane 3
2	SR_SCR_LN2	R/W		lane 2 scrambler reset
			0	**no action**
			1	soft_reset scrambler of lane 2
1	SR_SCR_LN1	R/W		lane 1 scrambler reset
			0	**no action**
			1	soft_reset scrambler of lane 1
0	SR_SCR_LN0	R/W		lane 0 scrambler reset
			0	**no action**
			1	soft_reset scrambler of lane 0

Table 83. Initialization values registers (address 11h to 1Ah) bit description

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
11h	INIT_SCR_S15T8_LN0	7 to 0	INIT_DESCR_LN0[15:8]	R/W	00h	initialization value for lane 0 descrambler bits s15 to s8
12h	INIT_SCR_S7T1_LN0	6 to 0	INIT_DESCR_LN0[[6:0]	R/W	00h	initialization value for lane 0 descrambler bits s7 to s1
13h	INIT_SCR_S15T8_LN1	7 to 0	INIT_DESCR_LN1[15:8]	R/W	00h	initialization value for lane 1 descrambler bits s15 to s8
14h	INIT_SCR_S7T1_LN1	6 to 0	INIT_DESCR_LN1[[6:0]	R/W	00h	initialization value for lane 1 descrambler bits s7 to s1
15h	INIT_SCR_S15T8_LN2	7 to 0	INIT_DESCR_LN2[15:8]	R/W	00h	initialization value for lane 2 descrambler bits s15 to s8
16h	INIT_SCR_S7T1_LN2	6 to 0	INIT_DESCR_LN2[[6:0]	R/W	00h	initialization value for lane 2 descrambler bits s7 to s1
17h	INIT_SCR_S15T8_LN3	7 to 0	INIT_DESCR_LN3[15:8]	R/W	00h	initialization value for lane 3 descrambler bits s15 to s8
18h	INIT_SCR_S7T1_LN3	6 to 0	INIT_DESCR_LN3[[6:0]	R/W	00h	initialization value for lane 3 descrambler bits s7 to s1
19h	INIT_ILA_BUFPTR_LN01	7 to 4	INIT_ILA_BUFPTR_LN1[3:0]	R/W	88h	initialization value for lane 1 ILA buffer pointer
		3 to 0	INIT_ILA_BUFPTR_LN0[3:0]	R/W	88h	initialization value for lane 0 ILA buffer pointer
1Ah	INIT_ILA_BUFPTR_LN23	7 to 4	INIT_ILA_BUFPTR_LN3[3:0]	R/W	88h	initialization value for lane 3 ILA buffer pointer
		3 to 0	INIT_ILA_BUFPTR_LN2[3:0]	R/W	88h	initialization value for lane 2 ILA buffer pointer

Table 84. ERROR_HANDLING register (address 1Bh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
6	NAD_ERR_CORR	R/W		frame assembler
			0	**not-in-table errors passed to frame assembler**
			1	nad (nit and disparity) errors passed to frame assembler
0	IGN_ERR	R/W		general error mode
			0	**no action**
			1	ignore disparity/nit-errors at lane-controller

Table 85. REINIT_CTRL register (address 1Ch) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	REINIT_ILA_LN3	R/W		lane 3, ila buffer out-of-range check
			0	**no action**
			1	lane 3 ila buffer out-of-range_error activates reinitialization
6	REINIT_ILA_LN2	R/W		lane 2, ila buffer out-of-range check
			0	**no action**
			1	lane 2 ila buffer out-of-range_error activates reinitialization
5	REINIT_ILA_LN1	R/W		lane 1, ila buffer out-of-range check
			0	**no action**
			1	lane 1 ila buffer out-of-range_error activates reinitialization
4	REINIT_ILA_LN0	R/W		lane 0, ila buffer out-of-range check
			0	**no action**
			1	lane 0 ila buffer out-of-range_error activates reinitialization
3	RESYNC_O_L_LN3	R/W		lane 3, resync over link
			0	**no action**
			1	lane 3 lane controller checks for K28.5 /K/ symbols
2	RESYNC_O_L_LN2	R/W		lane 2, resync over link
			0	**no action**
			1	lane 2 lane controller checks for K28.5 /K/ symbols
1	RESYNC_O_L_LN1	R/W		lane 1, resync over link
			0	**no action**
			1	lane 1 lane controller checks for K28.5 /K/ symbols
0	RESYNC_O_L_LN0	R/W		lane 0, resync over link
			0	**no action**
			1	lane 0 controller checks for K28.5 /K/ symbols

Table 86. MISC_CTRL register (address 1Dh) bit description

Bit	Symbol	Access	Value	Description
7	DLP-STROBE	R/W		captures the 8-bit data inside the DLP for each lane (see Table 110 and Table 116, 0E, 0F and 1E)
			0	no action
			1	update dlp sample
1 to 0	RESERVED[1:0]	R/W	-	reserved

Table 87. LMF_CTRL register (address 1Eh) bit description

Bit	Symbol	Access	Value	Description
7 to 5	L[2:0]	R/W	-	number of lanes [1, 2, 4]
4 to 3	M[1:0]	R/W	-	number of converters [1]
2 to 0	F[2:0]	R/W	-	number of octets/frame [1, 2, 4]

Table 88. PAGE_ADDRESS register (address 1Fh) bit description

Bit	Symbol	Access	Value	Description
4 to 0	PAGE[4:0]	R/W	0h	page_address

10.17.5 Page x04: RX digital lane processing monitoring

This page enables the monitoring of the digital lane processing, ensuring the data is decoded correctly. The validity of the link can also be tested by using simple Bit Error Rate testing and be monitored through various available flags and counters registers.

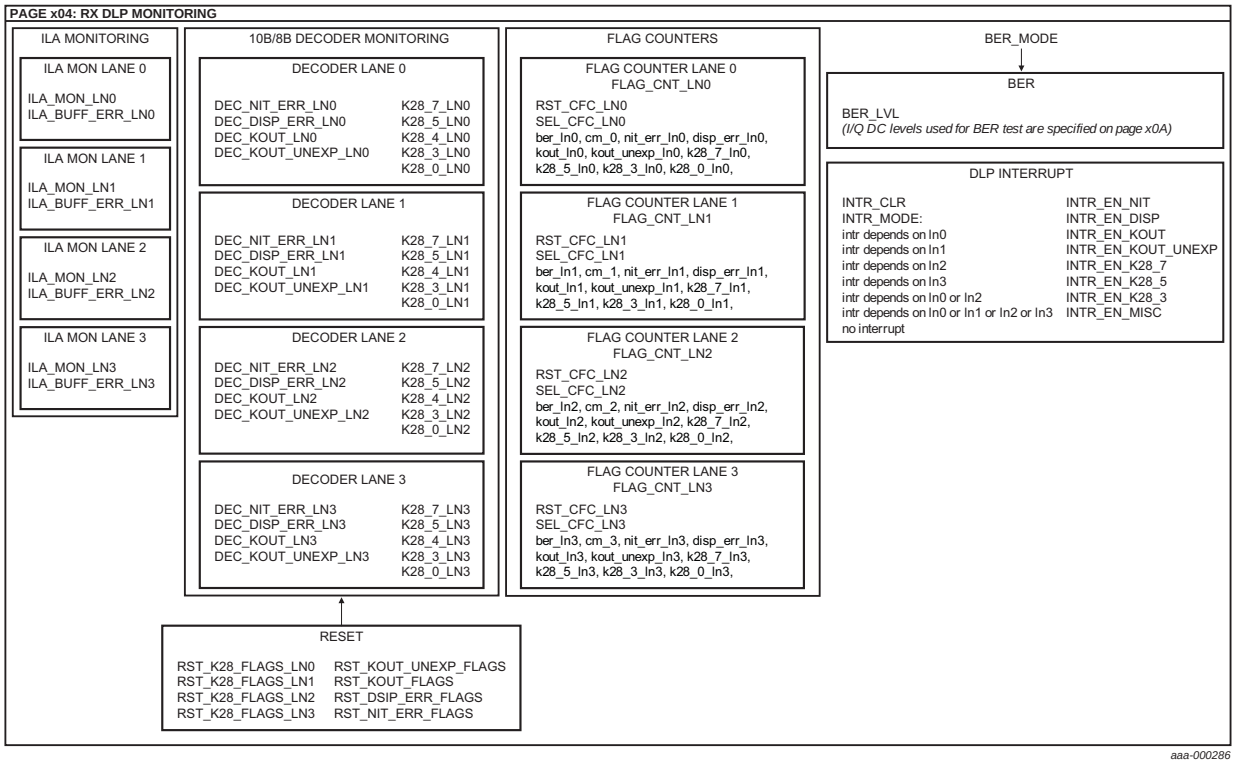


Fig 27. Page x04: RX digital lane processing monitoring

10.17.5.1 Page x04 allocation map description

Table 89 shows an overview of all registers on page x04.

Table 89. Page x04 register allocation map

Address		Register name	R/W	Bit definition								Default[1]	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
0	00h	ILA_MON_1_0	R	ILA_MON_LN1[3:0]				ILA_MON_LN0[3:0				uuuu uuuu	uuh
1	01h	ILA_MON_3_2	R	ILA_MON_LN3[3:0]				ILA_MON_LN2[3:0]				uuuu uuuu	uuh
2	02h	ILA_BUFF_ERR	R	-	-	-	-	ILA_BUFF_ERR_LN3	ILA_BUFF_ERR_LN2	ILA_BUFF_ERR_LN1	ILA_BUFF_ERR_LN0	uuuu uuuu	uuh
3	03h	CA_MON	R	CA_MON_LN3[1:0]		CA_MON_LN2[1:0]		CA_MON_LN1[1:0]		CA_MON_LN0[1:0]		uuuu uuuu	uuh
4	04h	DEC_FLAGS	R	DEC_NIT_ERR_LN3	DEC_NIT_ERR_LN2	DEC_NIT_ERR_LN1	DEC_NIT_ERR_LN0	DEC_DISP_ERR_LN3	DEC_DISP_ERR_LN2	DEC_DISP_ERR_LN1	DEC_DISP_ERR_LN0	uuuu uuuu	uuh
5	05h	KOUT_FLAG	R	-	-	-	-	DEC_KOUT_LN3	DEC_KOUT_LN2	DEC_KOUT_LN1	DEC_KOUT_LN0	uuuu uuuu	uuh
6	06h	K28_LN0_FLAG	R	-	-	-	K28_7_LN0	K28_5_LN0	K28_4_LN0	K28_3_LN0	K28_0_LN0	uuuu uuuu	uuh
7	07h	K28_LN1_FLAG	R	-	-	-	K28_7_LN1	K28_5_LN1	K28_4_LN1	K28_3_LN1	K28_0_LN1	uuuu uuuu	uuh
8	08h	K28_LN2_FLAG	R	-	-	-	K28_7_LN2	K28_5_LN2	K28_4_LN2	K28_3_LN2	K28_0_LN2	uuuu uuuu	uuh
9	09h	K28_LN3_FLAG	R	-	-	-	K28_7_LN3	K28_5_LN3	K28_4_LN3	K28_3_LN3	K28_0_LN3	uuuu uuuu	uuh
10	0Ah	KOUT_UNEXPECTED_FLAG	R	-	-	-	-	DEC_KOUT_UNEXP_LN3	DEC_KOUT_UNEXP_LN2	DEC_KOUT_UNEXP_LN1	DEC_KOUT_UNEXP_LN0	uuuu uuuu	uuh
11	0Bh	LOCK_CNT_MON_LN01	R	LOCK_CNT_MON_LN1[3:0]				LOCK_CNT_MON_LN0[3:0]				uuuu uuuu	uuh
12	0Ch	LOCK_CNT_MON_LN23	R	LOCK_CNT_MON_LN3[3:0]				LOCK_CNT_MON_LN2[3:0]				uuuu uuuu	uuh
13	0Dh	CS_STATE_LNX	R	CS_STATE_LN3[1:0]		CS_STATE_LN2[1:0]		CS_STATE_LN1[1:0]		CS_STATE_LN0[1:0]		uuuu uuuu	uuh
14	0Eh	MISC_FLAG_CTRL	R/W	RST_BUFF_ERR_FLAGS	AUTO_RST_FLAG_CNTS	HOLD_FLAG_CNT_EN	DUTY_MEAS_EN	DUTY_DLY_SEL[3:0]				0000 0000	00h

Table 89. Page x04 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default[1]	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
15	0Fh	INTR_MISC_EN	R/W	INTR_BUFF_EN_CS_INIT_LN3	INTR_EN_CS_INIT_LN2	INTR_EN_CS_INIT_LN1	INTR_EN_CS_INIT_LN0	INTR_EN_BUFF_ERR_LN3	INTR_EN_BUFF_ERR_LN2	INTR_EN_BUFF_ERR_LN1	INTR_EN_BUFF_ERR_LN0	0000 0000	00h
16	10h	FLAG_CNT_LSB_LN0	R	FLAG_CNT_LN0[7:0]								uuuu uuuu	uuh
17	11h	FLAG_CNT_MSB_LN0	R	FLAG_CNT_LN0[15:8]								uuuu uuuu	uuh
18	12h	FLAG_CNT_LSB_LN1	R	FLAG_CNT_LN1[7:0]								uuuu uuuu	uuh
19	13h	FLAG_CNT_MSB_LN1	R	FLAG_CNT_LN1[15:8]								uuuu uuuu	uuh
20	14h	FLAG_CNT_LSB_LN2	R	FLAG_CNT_LN2[7:0]								uuuu uuuu	uuh
21	15h	FLAG_CNT_MSB_LN2	R	FLAG_CNT_LN2[15:8]								uuuu uuuu	uuh
22	16h	FLAG_CNT_LSB_LN3	R	FLAG_CNT_LN3[7:0]								uuuu uuuu	uuh
23	17h	FLAG_CNT_MSB_LN3	R	FLAG_CNT_LN3[15:8]								uuuu uuuu	uuh
24	18h	BER_LVL_LSB	R/W	BER_LVL[7:0]								0000 0000	00h
25	19h	BER_LVL_MSB	R/W	BER_LVL[15:8]								0000 0000	00h
26	1Ah	INTR_EN	R/W	INTR_EN_NIT	INTR_EN_DISP	INTR_EN_KOUT	INTR_EN_KOUT_UNEXP	INTR_EN_K28_7	INTR_EN_K28_5	INTR_EN_K28_3	INTR_EN_MISC	0000 0000	00h
27	1Bh	CTRL_FLAG_CNT_LN10	R/W	RST_CFC_LN1	SEL_CFC_LN1[2:0]			RST_CFC_LN0	SEL_CFC_LN0[2:0]			0101 0101	55h
28	1Ch	CTRL_FLAG_CNT_LN32	R/W	RST_CFC_LN3	SEL_CFC_LN3[2:0]			RST_CFC_LN2	SEL_CFC_LN2[2:0]			0101 0101	55h

Table 89. Page x04 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default[1]	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
29	1Dh	MON_FLAGS_RST	R/W	RST_NIT_ERR-FLAGS	RST_DISP_ERR_FLAGS	RST_KOUT_FLAGS	RST_KOUT_UNEXP_FLAGS	RST_K28_LN3_FLAGS	RST_K28_LN2_FLAGS	RST_K28_LN1_FLAGS	RST_K28_LN0_FLAGS	0000 0000	00h
30	1Eh	DBG_CTRL	R/W	BER_MODE	INTR_CLR	INTR_MODE[2:0]			DBG_MODE[2:0]			0000 0000	00h
31	1Fh	PAGE_ADDRESS	R/W	-	-	-	PAGE[4:0]					0000 0000	00h

[1] u = undefined at power-up or after reset.

10.17.5.2 Page x04 bit definition detailed description

The tables in this section contain detailed descriptions of the page x04 registers.

Table 90. ILA_MON registers (address 00h to 01h) bit description

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
00h	ILA_MON_1_0	7 to 4	ILA_MON_LN1[3:0]	R	-	ila_buf_ln1 pointer
		3 to 0	ILA_MON_LN0[3:0]		-	ila_buf_ln0 pointer
01h	ILA_MON_3_2	7 to 4	ILA_MON_LN3[3:0]	R	-	ila_buf_ln3 pointer
		3 to 0	ILA_MON_LN2[3:0]		-	ila_buf_ln2 pointer

Table 91. ILA_BUFF_ERR register (address 02h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
3	ILA_BUFF_ERR_LN3	R		lane 3 ila buffer error
			0	ila_buf_ln3 pointer is in range
			1	ila_buf_ln3 pointer is out of range
2	ILA_BUFF_ERR_LN2	R		lane 2 ila buffer error
			0	ila_buf_ln2 pointer is in range
			1	ila_buf_ln2 pointer is out of range
1	ILA_BUFF_ERR_LN1	R		lane 1 ila buffer error
			0	ila_buf_ln1 pointer is in range
			1	ila_buf_ln1 pointer is out of range
0	ILA_BUFF_ERR_LN0	R		lane 0 ila buffer error
			0	ila_buf_ln0 pointer is in range
			1	ila_buf_ln0 pointer is out of range

Table 92. CA_MON register (address 03h) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	CA_MON_LN3[1:0]	R	-	clock alignment phase monitor lane 3
5 to 4	CA_MON_LN2[1:0]	R	-	clock alignment phase monitor lane 2
3 to 2	CA_MON_LN1[1:0]	R	-	clock alignment phase monitor lane 1
1 to 0	CA_MON_LN0[1:0]	R	-	clock alignment phase monitor lane 0

Table 93. DEC_FLAGS register (address 04h) bit description

Bit	Symbol	Access	Value	Description
7	DEC_NIT_ERR_LN3	R	-	not-in-table error flag lane 3
6	DEC_NIT_ERR_LN2	R	-	not-in-table error flag lane 2
5	DEC_NIT_ERR_LN1	R	-	not-in-table error flag lane 1
4	DEC_NIT_ERR_LN0	R	-	not-in-table error flag lane 0
3	DEC_DISP_ERR_LN3	R	-	disparity error flag lane 3
2	DEC_DISP_ERR_LN2	R	-	disparity error flag lane 2
1	DEC_DISP_ERR_LN1	R	-	disparity error flag lane 1
0	DEC_DISP_ERR_LN0	R	-	disparity error flag lane 0

Table 94. KOUT_FLAG register (address 05h) bit description

Bit	Symbol	Access	Value	Description
3	DEC_KOUT_LN3	R	-	/K/ symbols found in lane 3
2	DEC_KOUT_LN2	R	-	/K/ symbols found in lane 2
1	DEC_KOUT_LN1	R	-	/K/ symbols found in lane 1
0	DEC_KOUT_LN0	R	-	/K/ symbols found in lane 0

Table 95. K28 FLAG registers (address 06h to 09h) bit description

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
06h	K28_LN0_FLAG	4	K28_7_LN0	R	-	K28_7 /F/ symbols found in lane 0
		3	K28_5_LN0		-	K28_5 /K/ symbols found in lane 0
		2	K28_4_LN0		-	K28_4 /Q/ symbols found in lane 0
		1	K28_3_LN0		-	K28_3 /A/ symbols found in lane 0
		0	K28_0_LN0		-	K28_0 /R/ symbols found in lane 0
07h	K28_LN1_FLAG	4	K28_7_LN1	R	-	K28_7 /F/ symbols found in lane 1
		3	K28_5_LN1		-	K28_5 /K/ symbols found in lane 1
		2	K28_4_LN1		-	K28_4 /Q/ symbols found in lane 1
		1	K28_3_LN1		-	K28_3 /A/ symbols found in lane 1
		0	K28_0_LN1		-	K28_0 /R/ symbols found in lane 1
08h	K28_LN2_FLAG	4	K28_7_LN2	R	-	K28_7 /F/ symbols found in lane 2
		3	K28_5_LN2		-	K28_5 /K/ symbols found in lane 2
		2	K28_4_LN2		-	K28_4 /Q/ symbols found in lane 2
		1	K28_3_LN2		-	K28_3 /A/ symbols found in lane 2
		0	K28_0_LN2		-	K28_0 /R/ symbols found in lane 2
09h	K28_LN3_FLAG	4	K28_7_LN3	R	-	K28_7 /F/ symbols found in lane 3
		3	K28_5_LN3		-	K28_5 /K/ symbols found in lane 3
		2	K28_4_LN3		-	K28_4 /Q/ symbols found in lane 3
		1	K28_3_LN3		-	K28_3 /A/ symbols found in lane 3
		0	K28_0_LN3		-	K28_0 /R/ symbols found in lane 3

Table 96. KOUT_UNEXPECTED_FLAG register (address 0Ah) bit description

Bit	Symbol	Access	Value	Description
3	DEC_KOUT_UNEXP_LN3	R	-	unexpected /K/ symbols found in lane 3
2	DEC_KOUT_UNEXP_LN2	R	-	unexpected /K/ symbols found in lane 2
1	DEC_KOUT_UNEXP_LN1	R	-	unexpected /K/ symbols found in lane 1
0	DEC_KOUT_UNEXP_LN0	R	-	unexpected /K/ symbols found in lane 0

Table 97. LOCK_CNT_MON registers (address 0Bh to 0Ch) bit description

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0Bh	LOCK_CNT_MON_LN01	7 to 4	LOCK_CNT_MON_LN1[3:0]	R	-	lock_state monitor synchronization word alignment lane 1
		3 to 0	LOCK_CNT_MON_LN0[3:0]		-	lock_state monitor synchronization word alignment lane 0
0Ch	LOCK_CNT_MON_LN23	7 to 4	LOCK_CNT_MON_LN3[3:0]	R	-	lock_state monitor synchronization word alignment lane 3
		3 to 0	LOCK_CNT_MON_LN2[3:0]		-	lock_state monitor synchronization word alignment lane 2

Table 98. CS_STATE_LNX register (address 0Dh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 6	CS_STATE_LN3[1:0]	R	-	monitor cs_state fsm lane 3 (see Table 109)
5 to 4	CS_STATE_LN2[1:0]	R	-	monitor cs_state fsm lane 2 (see Table 109)
3 to 2	CS_STATE_LN1[1:0]	R	-	monitor cs_state fsm lane 1 (see Table 109)
1 to 0	CS_STATE_LN0[1:0]	R	-	monitor cs_state fsm lane 0 (see Table 109)

Table 99. RST_BUF_ERR_FLAGS register (address 0Eh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	RST_BUFF_ERR_FLAGS	R/W	0	reset ILA_BUF_ERR_LNx flags

Table 100. INTR_MISC_ENA register (address 0Fh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7	INTR_EN_CS_INIT_LN3	R/W	**0**	**no action**
			1	intr_misc in case cs_state_ln3 = cs_init
6	INTR_EN_CS_INIT_LN2	R/W	**0**	**no action**
			1	intr_misc in case cs_state_ln2 = cs_init
5	INTR_EN_CS_INIT_LN1	R/W	**0**	**no action**
			1	intr_misc in case cs_state_ln1 = cs_init
4	INTR_EN_CS_INIT_LN0	R/W	**0**	**no action**
			1	intr_misc in case cs_state_ln0 = cs_init
3	INTR_EN_BUF_ERR_LN3	R/W	**0**	**no action**
			1	generate interrupt if ILA_BUF_ERR_LN3 = 1

Table 100. INTR_MISC_ENA register (address 0Fh) bit description *...continued*

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
2	INTR_EN_BUF_ERR_LN2	R/W	**0**	**no action**
			1	generate interrupt if ILA_BUF_ERR_LN2 = 1
1	INTR_EN_BUF_ERR_LN1	R/W	**0**	**no action**
			1	generate interrupt if ILA_BUF_ERR_LN1 = 1
0	INTR_EN_BUF_ERR_LN0	R/W	**0**	**no action**
			1	generate interrupt if ILA_BUF_ERR_LN0 = 1

Table 101. LSB/MSB of flag_counter lane registers (address 10h to 17h) bit description

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
10h	FLAG_CNT_LSB_LN0	7 to 0	FLAG_CNT_LN0[7:0]	R	-	LSBs of flag counter lane 0
11h	FLAG_CNT_MSB_LN0	7 to 0	FLAG_CNT_LN0[15:8]	R	-	MSBs of flag_counter lane 0
12h	FLAG_CNT_LSB_LN1	7 to 0	FLAG_CNT_LN1[7:0]	R	-	LSBs of flag_counter lane 1
13h	FLAG_CNT_MSB_LN1	7 to 0	FLAG_CNT_LN1[15:8]	R	-	MSBs of flag_counter lane 1
14h	FLAG_CNT_LSB_LN2	7 to 0	FLAG_CNT_LN2[7:0]	R	-	LSBs of flag_counter lane 2
15h	FLAG_CNT_MSB_LN2	7 to 0	FLAG_CNT_LN2[15:8]	R	-	MSBs of flag_counter lane 2
16h	FLAG_CNT_LSB_LN3	7 to 0	FLAG_CNT_LN3[7:0]	R	-	LSBs of flag_counter lane 3
17h	FLAG_CNT_MSB_LN3	7 to 0	FLAG_CNT_LN3[15:8]	R	-	MSBs of flag_counter lane 3

Table 102. LSB/MSB BER measurement registers (address 18h to 19h) bit description

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
18h	BER_LVL_LSB	7 to 0	BER_LVL[7:0]	R/W	00h	LSBs level used for simple (DC) BER measurement
19h	BER_LVL_MSB	7 to 0	BER_LVL[15:8]	R/W	00h	MSBs level used for simple (DC) BER measurement

Table 103. INTR_ENA register (address 1Ah) bit description

Bit	Symbol	Access	Value	Description
7	INTR_EN_NIT	R/W		not-in-table interrupt
			0	**no action**
			1	nit_error impacts global interrupt as per INTR_MODE configuration (bit 1E)
6	INTR_EN_DISP	R/W		disparity-error interrupt
			0	**no action**
			1	disparity-error in ln<x> affects i_ln<x>
5	INTR_EN_KOUT	R/W		K-character interrupt
			0	**no action**
			1	detection k-control character in ln<x> affects i_ln<x>

Table 103. INTR_ENA register (address 1Ah) bit description *...continued*

Bit	Symbol	Access	Value	Description
4	INTR_EN_KOUT_UNEXP	R/W		unexpected K-character interrupt
			0	**no action**
			1	detection unexpected K-character in ln<x> affects i_ln<x>
3	INTR_EN_K28_7	R/W		K28_7 interrupt
			0	**no action**
			1	detection K28_7 in ln<x> affects i_ln<x>
2	INTR_EN_K28_5	R/W		K28_5 interrupt
			0	**no action**
			1	detection K28_5 in ln<x> affects i_ln<x>
1	INTR_EN_K28_3	R/W		K28_3 interrupt
			0	**no action**
			1	detection K28_3 in ln<x> affects i_ln<x>
0	INTR_EN_MISC	R/W		miscellaneous interrupt
			0	**no action**
			1	detection depends on intr_misc_ena (see Table 100)

Table 104. CTRL_FLAGCNT registers (address 1Bh to 1Ch) bit description

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
1Bh	CTRL_FLAG_CNT_LN10	7	RST_CFC_LN1	R/W	0	reset FLAG_CNT_LN1
		6 to 4	SEL_CFC_LN1[2:0]		5h	select FLAG_CNT_LN1 source (see Table 108)
		3	RST_CFC_LN0		0	reset FLAG_CNT_LN0
		2 to 0	SEL_CFC_LN0[2:0]		5h	select FLAG_CNT_LN0 source (see Table 108)
1Ch	CTRL_FLAG_CNT_LN32	7	RST_CFC_LN3	R/W	0	reset FLAG_CNT_LN3
		6 to 4	SEL_CFC_LN3[2:0]		5h	select FLAG_CNT_LN3 source (see Table 108)
		3	RST_CFC_LN2		0	reset FLAG_CNT_LN2
		2 to 0	SEL_CFC_LN2[2:0]		5h	select FLAG_CNT_LN2 source (see Table 108)

Table 105. MON_FLAGS_RESET register (address 1Dh) bit description

Bit	Symbol	Access	Value	Description
7	RST_NIT_ERR_FLAGS	R/W	0	reset nit-error monitor flags
6	RST_DISP_ERR_FLAGS	R/W	0	reset disparity monitor flags
5	RST_KOUT_FLAGS	R/W	0	reset K symbols monitor flags
4	RST_KOUT_UNEXPECTED_FLAGS	R/W	0	reset unexpected K symbols monitor flags
3	RST_K28_LN3_FLAGS	R/W	0	reset K28_x monitor flags for lane 3

Table 105. MON_FLAGS_RESET register (address 1Dh) bit description *...continued*

Bit	Symbol	Access	Value	Description
2	RST_K28_LN2_FLAGS	R/W	0	reset K28_x monitor flags for lane 2
1	RST_K28_LN1_FLAGS	R/W	0	reset K28_x monitor flags for lane 1
0	RST_K28_LN0_FLAGS	R/W	0	reset K28_x monitor flags for lane 0

Table 106. DBG_CNTRL register (address 1Eh) bit description

Bit	Symbol	Access	Value	Description
7	BER_MODE	R/W		simple BER-measurement
			0	**no action**
			1	simple BER measurement enabled
6	INTR_CLR	R/W		interrupts clear
			0	**no action**
			1	clear interrupts (to '1')
5 to 3	INTR_MODE[2:0]	R/W		interrupt settings
			000	**global interrupt depends on lane 0**
			001	global interrupt depends on lane 1
			010	global interrupt depends on lane 2
			011	global interrupt depends on lane 3
			100	global interrupt depends on lane 0 or lane 1
			101	global interrupt depends on lane 2 or lane 3
			110	global interrupt depends on lane 0 or lane 1 or lane 2 or lane 3
			111	no interrupt

Table 107. PAGE_ADDRESS register (address 1Fh) bit description

Bit	Symbol	Access	Value	Description
4 to 0	PAGE[4:0]	R/W	0h	page_address

Table 108. Counter source

Default settings are shown highlighted.

SEL_CFC_LNn[2:0]	Source
000	not-in-table error
001	disparity error
010	K symbol found
011	unexpected K symbol found
100	K28_7 (/F/) symbol found
101	K28_5 (/K/) symbol found
110	K28_3 (/A/) symbol found
111	K28_0 (/R/) symbol found

Table 109. Code group synchronization state machine

CS_STATE_LNn[1:0]	Definition
00	looking for K28_5 (/K/) symbol
01	four consecutive K28_5 (/K/) symbols have been received
10	code group synchronization achieved
11	not applicable

10.17.6 Page x08/x09: JESD204 read configuration

These two pages reproduce the values of the configuration data transmitted from the TX in the second multiframe of the inter-lane alignment sequence and decoded in the DAC1628D1G25.

PAGE x08: JESD204 READ CONFIGURATION

LANE 0 JESD204 CONFIGURATION

CONFIG 0	LN0_DID	
CONFIG 1	LN0_ADJCNT	LN0_BID
CONFIG 2	LN0_ADJDIR LN0_PHADJ	LN0_LID
CONFIG 3	LN0_SCR	LN0_L
CONFIG 4	LN0_F	
CONFIG 5		LN0_K
CONFIG 6	LN0_M	
CONFIG 7	LN0_CS	LN0_N
CONFIG 8	LN0_SUBCLASSV	LN0_N'
CONFIG 9	LN0_JESDV	LN0_S
CONFIG 10	LN0_HD	LN0_CF
CONFIG 11	LN0_RES1	
CONFIG 12	LN0_RES2	
CONFIG 13	LN0_FCHK	

LANE 1 JESD204 CONFIGURATION

CONFIG 0	LN1_DID	
CONFIG 1	LN1_ADJCNT	LN1_BID
CONFIG 2	LN1_ADJDIR LN1_PHADJ	LN1_LID
CONFIG 3	LN1_SCR	LN1_L
CONFIG 4	LN1_F	
CONFIG 5		LN1_K
CONFIG 6	LN1_M	
CONFIG 7	LN1_CS	LN1_N
CONFIG 8	LN1_SUBCLASSV	LN1_N'
CONFIG 9	LN1_JESDV	LN1_S
CONFIG 10	LN1_HD	LN1_CF
CONFIG 11	LN1_RES1	
CONFIG 12	LN1_RES2	
CONFIG 13	LN1_FCHK	

aaa-000287

Fig 28. Page x08: JESD204 read configuration

PAGE x09: JESD204 READ CONFIGURATION

LANE 2 JESD204 CONFIGURATION

CONFIG 0	LN2_DID	
CONFIG 1	LN2_ADJCNT	LN2_BID
CONFIG 2	LN2_ADJDIR LN2_PHADJ	LN2_LID
CONFIG 3	LN2_SCR	LN2_L
CONFIG 4	LN2_F	
CONFIG 5		LN2_K
CONFIG 6	LN2_M	
CONFIG 7	LN2_CS	LN2_N
CONFIG 8	LN2_SUBCLASSV	LN2_N'
CONFIG 9	LN2_JESDV	LN2_S
CONFIG 10	LN2_HD	LN2_CF
CONFIG 11	LN2_RES1	
CONFIG 12	LN2_RES2	
CONFIG 13	LN2_FCHK	

LANE 3 JESD204 CONFIGURATION

CONFIG 0	LN3_DID	
CONFIG 1	LN3_ADJCNT	LN3_BID
CONFIG 2	LN3_ADJDIR LN3_PHADJ	LN3_LID
CONFIG 3	LN3_SCR	LN3_L
CONFIG 4	LN3_F	
CONFIG 5		LN3_K
CONFIG 6	LN3_M	
CONFIG 7	LN3_CS	LN3_N
CONFIG 8	LN3_SUBCLASSV	LN3_N
CONFIG 9	LN3_JESDV	LN3_S
CONFIG 10	LN3_HD	LN3_CF
CONFIG 11	LN3_RES1	
CONFIG 12	LN3_RES2	
CONFIG 13	LN3_FCHK	

aaa-000288

Fig 29. Page x09: JESD204 read configuration

10.17.6.1 Page x08 allocation map

Table 110 shows an overview of all registers on page x08.

Table 110. Page x08 register allocation map

Address		Register name	R/W	Bit definition								Default[1]	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
0	00h	LN0_CFG_0	R	LN0_DID[7:0]								uuuu uuuu	uuh
1	01h	LN0_CFG_1	R	LN0_ADJCNT[3:0]				LN0_BID[3:0]				uuuu uuuu	uuh
2	02h	LN0_CFG_2	R	-	LN0_ ADJDIR	LN0_ PHADJ	LN0_LID[4:0]					uuuu uuuu	uuh
3	03h	LN0_CFG_3	R	LN0_SCR	-	-	LN0_L[4:0]					uuuu uuuu	uuh
4	04h	LN0_CFG_4	R	LN0_F[7:0]								uuuu uuuu	uuh
5	05h	LN0_CFG_5	R	-	-	-	LN0_K[4:0]					uuuu uuuu	uuh
6	06h	LN0_CFG_6	R	LN0_M[7:0]								uuuu uuuu	uuh
7	07h	LN0_CFG_7	R	LN0_CS[1:0]		-	LN0_N[4:0]					uuuu uuuu	uuh
8	08h	LN0_CFG_8	R	LN0_SUBCLASSV[2:0]			LN0_N'[4:0]					uuuu uuuu	uuh
9	09h	LN0_CFG_9	R	LN0_JESDV[2:0]			LN0_S[4:0]					uuuu uuuu	uuh
10	0Ah	LN0_CFG_10	R	LN0_HD	-	-	LN0_CF[4:0]					uuuu uuuu	uuh
11	0Bh	LN0_CFG_11	R	LN0_RES1[7:0]								uuuu uuuu	uuh
12	0Ch	LN0_CFG_12	R	LN0_RES2[7:0]								uuuu uuuu	uuh
13	0Dh	LN0_CFG_13	R	LN0_FCHK[7:0]								uuuu uuuu	uuh
14	0Eh	LN10_SAMPLE_ LSB	R	LN10_SAMPLE[7:0								uuuu uuuu	uuh

Table 110. Page x08 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default[1]	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
15	0Fh	LN10_SAMPLE_MSB	R	LN10_SAMPLE[15:8]								uuuu uuuu	uuh
16	10h	LN1_CFG_0	R	LN1_DID[7:0]								uuuu uuuu	uuh
17	11h	LN1_CFG_1	R	LN1_ADJCNT[3:0]				LN1_BID[3:0]				uuuu uuuu	uuh
18	12h	LN1_CFG_2	R	-	LN1_ADJDIR	LN1_PHADJ	LN1_LID[4:0]					uuuu uuuu	uuh
19	13h	LN1_CFG_3	R	LN1_SCR	-	-	LN1_L[4:0]					uuuu uuuu	uuh
20	14h	LN1_CFG_4	R	LN1_F[7:0]								uuuu uuuu	uuh
21	15h	LN1_CFG_5	R	-	-	-	LN1_K[4:0]					uuuu uuuu	uuh
22	16h	LN1_CFG_6	R	LN1_M[7:0]								uuuu uuuu	uuh
23	17h	LN1_CFG_7	R	LN1_CS[1:0]		-	LN1_N[4:0]					uuuu uuuu	uuh
24	18h	LN1_CFG_8	R	LN1_SUBCLASSV[2:0]			LN1_N'[4:0]					uuuu uuuu	uuh
25	19h	LN1_CFG_9	R	LN1_JESDV[2:0]			LN1_S[4:0]					uuuu uuuu	uuh
26	1Ah	LN1_CFG_10	R	LN1_HD	-	-	LN1_CF[4:0]					uuuu uuuu	uuh
27	1Bh	LN1_CFG_11	R	LN1_RES1[7:0]								uuuu uuuu	uuh
28	1Ch	LN1_CFG_12	R	LN1_RES2[7:0]								uuuu uuuu	uuh

Table 110. Page x08 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default[1]	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
29	1Dh	LN1_CFG_13	R	LN1_FCHK[7:0]								uuuu uuuu	uuh
30	1Eh	LN10_SEL	W	LN10_SEL[7:0]								0000 0000	00h
31	1Fh	PAGE_ADDRESS	R/W	-	-	-	PAGE[4:0]					0000 0000	00h

[1] u = undefined at power-up or after reset.

10.17.6.2 Page x08 bit definition detailed description

The tables in this section contain detailed descriptions of the page x08 registers.

Table 111. Lane 0 configuration registers (address 00h to 0Dh) bit description

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
00h	LN0_CFG_0	7 to 0	LN0_DID[7:0]	R	-	lane 0 device ID
01h	LN0_CFG_1	7 to 4	LN0_ADJCNT[3:0]	R	-	lane 0 adjustable counter
		3 to 0	LN0_BID[3:0]		-	lane 0 bank ID
02h	LN0_CFG_2	4 to 0	LN0_LID[4:0]	R	-	lane 0 lane ID
03h	LN0_CFG_3	6	LN0_ADJDIR	R	-	lane 0 adjustable direction
		5	LN0_PHADJ			lane 0 adjustable phase
		4 to 0	LN0_L[4:0]		-	number of lanes minus 1
04h	LN0_CFG_4	7 to 0	LN0_F[7:0]	R	-	number of octets per frame minus 1
05h	LN0_CFG_5	4 to 0	LN0_K[4:0]	R	-	number of frames per multi-frame minus 1
06h	LN0_CFG_6	7 to 0	LN0_M[7:0]	R	-	number of converters per device minus 1
07h	LN0_CFG_7	7 to 6	LN0_CS[1:0]	R	-	number of control bits
		4 to 0	LN0_N[4:0]		-	converter resolution minus 1
08h	LN0_CFG_8	7 to 5	LN0_SUBCLASSV[2:0]	R	-	lane 0 JSED204B subclass version
					00	subclass 0
					01	subclass 1
					10	subclass 2
		4 to 0	LN0_N'[4:0]	R	-	number of bits per sample minus 1
09h	LN0_CFG_9	7 to 5	LN0_JESDV	R	-	Lane 0 JESD204 version
					000	version A
					001	version B
		4 to 0	LN0_S[4:0]	R	-	number of samples per converter per frame cycle minus 1
0Ah	LN0_CFG_10	7	LN0_HD	R	-	high density
		4 to 0	LN0_CF[4:0]		-	number of control words per frame cycle
0Bh	LN0_CFG_11	7 to 0	LN0_RES1[7:0]	R	-	lane 0 reserved field
0Ch	LN0_CFG_12	7 to 0	LN0_RES2[7:0]	R	-	lane 0 reserved field
0Dh	LN0_CFG_13	7 to 0	LN0_FCHK[7:0]	R	-	lane 0 checksum

Table 112. Lane 1/lane 0 sample LSB/MSB registers (address 0Eh to 0Fh) bit description

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0Eh	LN10_SAMPLE_LSB	7 to 0	LN10_SAMPLE[7:0]	R	-	internal DLP data on lane 0 or lane 1 depending on the value of LN10_SELECT (bit 1E; LSB) The data are strobed by DLP_STROBE (see Table 89, bit 1D).
0Fh	LN10_SAMPLE[15:8]	7 to 0	LN10_SAMPLE[15:8]	R	-	internal DLP data on lane 0 or lane 1 depending on the value of LN10_SELECT (bit 1E; MSB) The data are strobed by DLP_STROBE (see Table 89, bit 1D).

Table 113. Lane 1 configuration registers (address 10h to 1Dh) bit description

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
10h	LN1_CFG_0	7 to 0	LN1_DID[7:0]	R	-	lane 1 device ID
11h	LN1_CFG_1	7 to 4	LN1_ADJCNT[3:0]	R	-	lane 1 adjustable counter
		3 to 0	LN1_BID[3:0]		-	lane 1 bank ID
12h	LN1_CFG_2	6	LN1_ADJDIR	R	-	lane 1 adjustable direction
		5	LN1_PHADJ		-	lane 1 adjustable phase
		4 to 0	LN1_LID[4:0]		-	lane 1 lane ID
13h	LN1_CFG_3	7	LN1_SCR	R	-	scrambling on
		4 to 0	LN1_L[4:0]		-	number of lanes minus 1
14h	LN1_CFG_4	7 to 0	LN1_F[7:0]	R	-	number of octets per frame minus 1
15h	LN1_CFG_5	4 to 0	LN1_K[4:0]	R	-	number of frames per multi-frame minus 1
16h	LN1_CFG_6	7 to 0	LN1_M[7:0]	R	-	number of converters per device minus 1
17h	LN1_CFG_7	7 to 6	LN1_CS[1:0]	R	-	number of control bits
		4 to 0	LN1_N[4:0]		-	converter resolution minus 1
18h	LN1_CFG_8	7 to 5	LN1_SUBCLASSV[2:0]	R	-	lane 1 JSED204B subclass version
					00	subclass 0
					01	subclass 1
					10	subclass 2
		4 to 0	LN1_N'[4:0]	R	-	number of bits per sample minus 1
19h	LN1_CFG_9	7 to 5	LN1_JESDV	R	-	Lane 1 JESD204 version
					000	version A
					001	version B
		4 to 0	LN1_S[4:0]	R	-	number of samples per converter per frame cycle minus 1

Table 113. Lane 1 configuration registers (address 10h to 1Dh) bit description *…continued*

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
1Ah	LN1_CFG_10	7	LN1_HD	R	-	high density
		4 to 0	LN1_CF[4:0]		-	number of control words per frame cycle
1Bh	LN1_CFG_11	7 to 0	LN1_RES1[7:0]	R	-	lane 1 reserved field
1Ch	LN1_CFG_12	7 to 0	LN1_RES2[7:0]	R	-	lane 1 reserved field
1Dh	LN1_CFG_13	7 to 0	LN1_FCHK[7:0]	R	-	lane 1 checksum

Table 114. LN10_SELECT register (address 1Eh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	LN10_SEL	W		specifies the lane affected by DLP_STROBE
			0	lane 0
			1	lane 1

Table 115. PAGE_ADDRESS register (address 1Fh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
4 to 0	PAGE[4:0]	R/W	0h	page_address

10.17.6.3 Page x09 allocation map description

Table 116 shows an overview of all registers on page x09.

Table 116. Page x09 register allocation map

Address		Register name	R/W	Bit definition								Default[1]	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
0	00h	LN2_CFG_0	R	LN2_DID[7:0]								uuuu uuuu	uuh
1	01h	LN2_CFG_1	R	LN2_ADJCNT[3:0]				LN2_BID[3:0]				uuuu uuuu	uuh
2	02h	LN2_CFG_2	R	-	LN2_ ADJDIR	LN2_ PHADJ	LN2_LID[4:0]					uuuu uuuu	uuh
3	03h	LN2_CFG_3	R	LN2_SCR	-	-	LN2_L[4:0]					uuuu uuuu	uuh
4	04h	LN2_CFG_4	R	LN2_F[7:0]								uuuu uuuu	uuh
5	05h	LN2_CFG_5	R	-	-	-	LN2_K[4:0]					uuuu uuuu	uuh
6	06h	LN2_CFG_6	R	LN2_M[7:0]								uuuu uuuu	uuh
7	07h	LN2_CFG_7	R	LN2_CS[1:0]		-	LN2_N[4:0]					uuuu uuuu	uuh
8	08h	LN2_CFG_8	R	LN2_SUBCLASSV[2:0]			LN2_N'[4:0]					uuuu uuuu	uuh
9	09h	LN2_CFG_9	R	LN2_JESDV[2:0]			LN2_S[4:0]					uuuu uuuu	uuh
10	0Ah	LN2_CFG_10	R	LN2_HD	-	-	LN2_CF[4:0]					uuuu uuuu	uuh
11	0Bh	LN2_CFG_11	R	LN2_RES1[7:0]								uuuu uuuu	uuh
12	0Ch	LN2_CFG_12	R	LN2_RES2[7:0]								uuuu uuuu	uuh
13	0Dh	LN2_CFG_13	R	LN2_FCHK[7:0]								uuuu uuuu	uuh
14	0Eh	LN32_SAMPLE_ LSB	R	LN32_SAMPLE[7:0]								uuuu uuuu	uuh

Table 116. Page x09 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default[1]	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
15	0Fh	LN32_SAMPLE_MSB	R	LN32_SAMPLE[15:8]									
16	10h	LN3_CFG_0	R	LN3_DID[7:0]								uuuu uuuu	uuh
17	11h	LN3_CFG_1	R	LN3_ADJCNT[3:0]				LN3_BID[3:0]				uuuu uuuu	uuh
18	12h	LN3_CFG_2	R	-	LN3_ADJDIR	LN3_PHADJ	LN3_LID[4:0]					uuuu uuuu	uuh
19	13h	LN3_CFG_3	R	LN3_SCR	-	-	LN3_L[4:0]					uuuu uuuu	uuh
20	14h	LN3_CFG_4	R	LN3_F[7:0]								uuuu uuuu	uuh
21	15h	LN3_CFG_5	R	-	-	-	LN3_K[4:0]					uuuu uuuu	uuh
22	16h	LN3_CFG_6	R	LN3_M[7:0]								uuuu uuuu	uuh
23	17h	LN3_CFG_7	R	LN3_CS[1:0]		-	LN3_N[4:0]					uuuu uuuu	uuh
24	18h	LN3_CFG_8	R	LN3_SUBCLASSV[2:0]			LN3_N'[4:0]					uuuu uuuu	uuh
25	19h	LN3_CFG_9	R	LN3_JESDV[2:0]			LN3_S[4:0]					uuuu uuuu	uuh
26	1Ah	LN3_CFG_10	R	LN3_HD	-	-	LN3_CF[4:0]					uuuu uuuu	uuh
27	1Bh	LN3_CFG_11	R	LN3_RES1[7:0]								uuuu uuuu	uuh
28	1Ch	LN3_CFG_12	R	LN3_RES2[7:0]								uuuu uuuu	uuh

Table 116. Page x09 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default[1]	
				b7	b6	b5	b4	b3	b2	b1	b0	Bin	Hex
29	1Dh	LN3_CFG_13	R	LN3_FCHK[7:0]								uuuu uuuu	uuh
30	1Eh	LN32_SELECT	W	LN32_SEL[7:0]								0000 0000	00h
31	1Fh	PAGE_ADDRESS	R/W	-	-	-	-	-	PAGE[2:0]			0000 0000	00h

[1] u = undefined at power-up or after reset.

10.17.6.4 Page x09 bit definition detailed description

The tables in this section contain detailed descriptions of the page x09 registers.

Table 117. Lane 2 configuration registers (address 10h to 1Dh) bit description

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
00h	LN2_CFG_0	7 to 0	LN2_DID[7:0]	R	-	lane 2 device ID
01h	LN2_CFG_2	7 to 4	LN2_ADJCNT[3:0]	R	-	lane 2 adjustable counter
		3 to 0	LN2_BID[3:0]		-	lane 2 bank ID
02h	LN2_CFG_2	6	LN2_ADJDIR	R	-	lane 2 adjustable direction
		5	LN2_PHADJ		-	lane 2 adjustable phase
		4 to 0	LN2_LID[4:0]		-	lane 2 lane ID
03h	LN2_CFG_3	7	LN2_SCR	R	-	scrambling on
		4 to 0	LN2_L[4:0]		-	number of lanes minus 1
04h	LN2_CFG_4	7 to 0	LN2_F[7:0]	R	-	number of octets per frame minus 1
05h	LN2_CFG_5	4 to 0	LN2_K[4:0]	R	-	number of frames per multi-frame minus 1
06h	LN2_CFG_6	7 to 0	LN2_M[7:0]	R	-	number of converters per device minus 1
07h	LN2_CFG_7	7 to 6	LN2_CS[1:0]	R	-	number of control bits
		4 to 0	LN2_N[4:0]		-	converter resolution minus 1
08h	LN2_CFG_8	7 to 5	LN2_SUBCLASSV[2:0]	R	-	lane 2 JSED204B subclass version
					00	subclass 0
					01	subclass 1
					10	subclass 2
		4 to 0	LN2_N'[4:0]	R	-	number of bits per sample minus 1
09h	LN2_CFG_9	7 to 5	LN2_JESDV	R	-	Lane 2 JESD204 version
					000	version A
					001	version B
		4 to 0	LN2_S[4:0]	R	-	number of samples per converter per frame cycle minus 1
0Ah	LN2_CFG_10	7	LN2_HD	R	-	high density
		4 to 0	LN2_CF[4:0]		-	number of control words per frame cycle
0Bh	LN2_CFG_11	7 to 0	LN2_RES1[7:0]	R	-	lane 2 reserved field
0Ch	LN2_CFG_12	7 to 0	LN2_RES2[7:0]	R	-	lane 2 reserved field
0Dh	LN2_CFG_13	7 to 0	LN2_FCHK[7:0]	R	-	lane 2 checksum

Table 118. Lane 3/lane 2 sample LSB/MSB registers (address 0Eh to 0Fh) bit description

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0Eh	LN32_SAMPLE_LSB	7 to 0	LN32_SAMPLE[7:0]	R	-	internal DLP data on lane 2 or lane 3 depending on the value of LN10_SELECT (bit 1E; LSB) The data are strobed by DLP_STROBE (see Table 89, bit 1D).
0Fh	LN32_SAMPLE[15:8]	7 to 0	LN32_SAMPLE[15:8]	R	-	internal DLP data on lane 2 or lane 3 depending on the value of LN10_SELECT (bit 1E; MSB) The data are strobed by DLP_STROBE (see Table 89, bit 1D).

Table 119. Lane 3 configuration registers (address 10h to 1Dh) bit description

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
10h	LN3_CFG_0	7 to 0	LN3_DID[7:0]	R	-	lane 3 device ID
11h	LN3_CFG_1	7 to 4	LN3_ADJCNT[3:0]	R	-	lane 3 adjustable counter
		3 to 0	LN3_BID[3:0]		-	lane 3 bank ID
12h	LN3_CFG_2	6	LN3_ADJDIR	R	-	lane 3 adjustable direction
		5	LN3_PHADJ		-	lane 3 adjustable phase
		4 to 0	LN3_LID[4:0]		-	lane 3 lane ID
13h	LN3_CFG_3	7	LN3_SCR	R	-	scrambling on
		4 to 0	LN3_L[4:0]		-	number of lanes minus 1
14h	LN3_CFG_4	7 to 0	LN3_F[7:0]	R	-	number of octets per frame minus 1
15h	LN3_CFG_5	4 to 0	LN3_K[4:0]	R	-	number of frames per multi-frame minus 1
16h	LN3_CFG_6	7 to 0	LN3_M[7:0]	R	-	number of converters per device minus 1
17h	LN3_CFG_7	7 to 6	LN3_CS[1:0]	R	-	number of control bits
		4 to 0	LN3_N[4:0]		-	converter resolution minus 1
18h	LN3_CFG_8	7 to 5	LN3_SUBCLASSV[2:0]	R	-	lane 3 JSED204B subclass version
					00	subclass 0
					01	subclass 1
					10	subclass 2
		4 to 0	LN3_N'[4:0]	R	-	number of bits per sample minus 1
19h	LN3_CFG_9	7 to 5	LN3_JESDV	R	-	Lane 3 JESD204 version
					000	version A
					001	version B
		4 to 0	LN3_S[4:0]	R	-	number of samples per converter per frame cycle minus 1

Table 119. Lane 3 configuration registers (address 10h to 1Dh) bit description *…continued*

Default settings are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
1Ah	LN3_CFG_10	7	LN3_HD	R	-	high density
		4 to 0	LN3_CF[4:0]		-	number of control words per frame cycle
1Bh	LN3_CFG_11	7 to 0	LN3_RES1[7:0]	R	-	lane 3 reserved field
1Ch	LN3_CFG_12	7 to 0	LN3_RES2[7:0]	R	-	lane 3 reserved field
1Dh	LN3_CFG_13	7 to 0	LN3_FCHK[7:0]	R	-	lane 3 checksum

Table 120. LN32_SELECT register (address 1Eh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	LN32_SEL	W		specifies the lane affected by DLP_STROBE
			0	lane 2
			1	lane 3

Table 121. PAGE_ADDRESS register (address 1Fh) bit description

Default settings are shown highlighted.

Bit	Symbol	Access	Value	Description
4 to 0	PAGE[4:0]	R/W	0h	page_address

10.17.7 Page x0A: Main controls

This page specifies the main configuration of the different clocking systems used in the DAC1628D1G25.

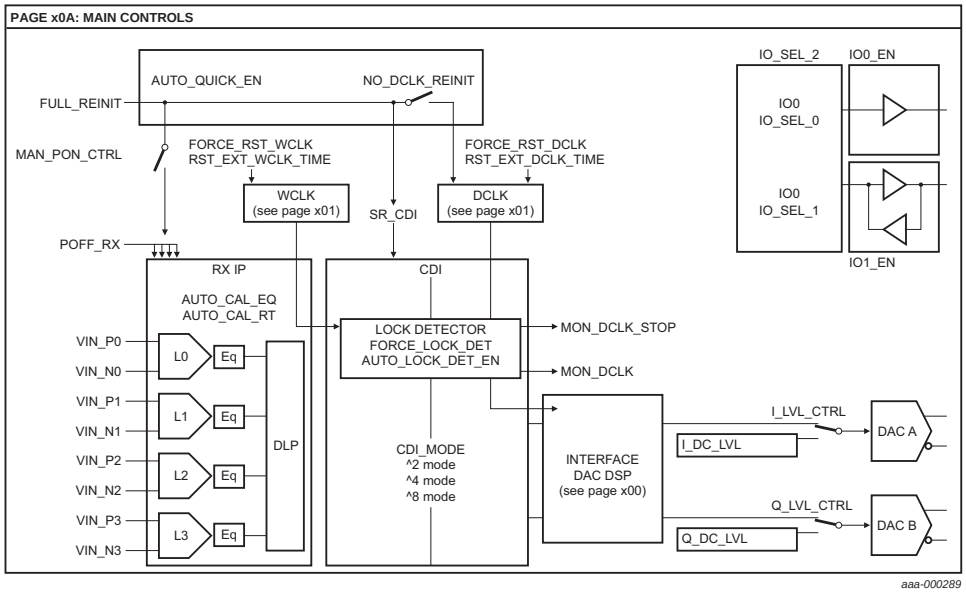


Fig 30. Page x0A: Main controls

10.17.7.1 Page x0A register allocation map

Table 122 shows an overview of all registers on page x0A.

Table 122. Page_x0A register allocation map

Address		Register name	R/W	Bit definition								Default	
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
0	00h	MAIN_CTRL	R/W	POFF_RX[3:0]				NO_DCLK_REINIT	FULL_REINIT	FORCE_RST_DCLK	FORCE_RST_WCLK	0000 0011	03h
1	01h	DCSMU_AUTO_CTRL	R/W	MAN_PON_CTRL	-	-	FORCE_LOCK_DET	AUTO_QUICK_EN	AUTO_LOCK_DET_EN	RESERVED	AUTO_CAL_EQ	0000 1100	0Ch
2	02h	DCSMU_AUTO_RT	R/W	-	-	-	-	-	-	RESERVED	AUTO_CAL_RT	0000 0000	00h
4	04h	RST_EXT_WCLK	R/W	RST_EXT_WCLK_TIME[7:0]								0100 0000	40h
5	05h	RST_EXT_DCLK	R/W	RST_EXT_DCLK_TIME[7:0]								0100 0000	40h
6	06h	DCMSU_PREDIVCNT	R/W	DCMSU_PREDIVIDER[7:0]								0001 0000	10h
7	07h	EHS_CTRL	R/W	-	-	IO_EN[1:0]		IO_EHS[1:0]		SDO_EHS[1:0]		0001 1010	1Ah
11	0Bh	MISC_CTRL	R/W	SR_CDI	RING_OSC_TEST	I_LVL_CTRL[1:0]		Q_LEV_CTRL[1:0]		CDI_MODE[1:0]		0000 0000	00h
12	0Ch	I_DC_LVL_LSB	R/W	I_DC_LVL[7:0]								0000 0000	00h
13	0Dh	I_DC_LVL_MSB	R/W	I_DC_LVL[15:8]								1000 0000	80h
14	0Eh	Q_DC_LVL_LSB	R/W	Q_DC_LVL[7:0]								0000 0000	00h
15	0Fh	Q_DC_LVL_MSB	R/W	Q_DC_LVL[15:8]								1000 0000	80h
16	10h	IO_MUX_CTRL0	R/W	IO_SEL_0[7:0]								1111 1111	FFh
17	11h	IO_MUX_CTRL1	R/W	IO_SEL_1[7:0]								1111 1111	FFh
18	12h	IO_MUX_CTRL2	R/W	IO_SEL_2[7:0]								1111 1111	FFh

Table 122. Page_x0A register allocation map *...continued*

Address		Register name	R/W	Bit definition								Default	
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
20	14h	MON_DCLK	R	MON_DCLK_STOP	-	-	-	MON_DCLK[3:0]				uuuu uuuu	uuh
21	15h	MON_DCLK_FLAGS	R	MON_DCLK_FLAGS[7:0]								uuuu uuuu	uuh
27	1Bh	TYPE_ID_0	R	TYPE_ID_0[7:0]								0101 1100	5Ch
28	1Ch	TYPE_ID_1	R	TYPE_ID_1[7:0]								0000 0001	01h
29	1Dh	TYPE_ID_2	R	TYPE_ID_2[7:0]								0000 0001	01h
30	1Eh	TYPE_ID_3	R	TYPE_ID_3[7:0]								0000 0001	01h
31	1Fh	PAGE_ADDRESS	R/W	-	-	-	PAGE[4:0]					0000 0000	00h

10.17.7.2 Page x0A bit definition detailed description

The tables in this section contain detailed descriptions of the page x0A registers.

Table 123. Register MAIN_CTRL (address 00h)

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	POFF_RX[3:0]	R/W	-	power-down of the physical lane receiver
				bit 7 = lane 3
				bit 6 = lane 2
				bit 5 = lane 1
				bit 4 = lane 0
3	NO_DCLK_REINIT	R/W		reinitialization, digital clock select
			0	full reinitialization with restart digital clock reset
			1	full reinitialization without restart digital clock reset
2	FULL_REINIT	R/W		quick/full reinitialization selection
			0	quick reinitialization
			1	full reinitialization
1	FORCE_RST_DCLK	R/W		digital clock reset
			0	release digital clock reset
			1	force digital clock reset
0	FORC_RST_WCLK	R/W		work clock reset
			0	release work clock reset
			1	force work clock reset

Table 124. Register DCSMU_AUTO_CTRL (address 01h)

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7	MAN_PON_CTRL	R/W		DCSMU auto-control
			0	pon_rx-phy and pon_dacs controlled by DCSMU
			1	manual control of pon_rx_phy and pon_dacs
4	FORCE_LOCK_DET	R/W		lock detection
			0	no action
			1	ignore internal lock detectors
3	AUTO_QUICK_EN	R/W		automatic control of the rx-phy power-up
			0	do not enable rx-phy after power-up/spi-reset
			1	enable rx-phy after power-up/spi-reset
2	AUTO_LOCK_DET_EN	R/W		automatic lock detection
			0	disabled
			1	enabled
1	RESERVED	R/W	-	reserved
0	AUTO_CAL_EQ	R/W		automatic calibration equalizer
			0	disabled (use auto-zero)
			1	enabled

Table 125. DCSMU_AUTO_RT (address 02h)
Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
1	RESERVED	R/W	0	reserved
0	AUTO_CAL_RT	R/W		autocalibration termination resistance
			0	disabled
			1	enabled

Table 126. Clock extension registers (address 04h to 05h) bit description
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
04h	RST_EXT_WCLK	7 to 0	RST_EXT_WCLK_TIME[7:0]	R/W		specify extension time reset, expressed in WCLK clock period
					-	8 bits for the extension time reset
05h	RST_EXT_DCLK	7 to 0	RST_EXT_DCLK_TIME[7:0]	R/W		specify extension time reset, expressed in DCLK period
					-	8 bits for the extension time reset

Table 127. Register DCSMU_PREDIV (address 06h)
Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	DCMSU_PREDIVIDER[7:0]	R/W		predivider value for the DCMSU, expressed in WCLK clock period
			-	8 bits for the predivider value

Table 128. Register MISC_CTRL (address 0Bh)
Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7	SR_CDI	R/W		CDI block software reset control
			0	**no action**
			1	perform a software reset on CDI
6	RESERVED	R/W	0	reserved
5 to 4	I_LEV_CTRL[1:0]	R/W		specifies output from CDI for I path
			00	**normal operation (CDI data output sent to digital signal processing input)**
			01	id data enable = 1: the normal operation; if data enable = 0: digital signal processing input = I_DC_LVL register value
			10	digital signal processing input = I_DC_LVL
			11	digital signal processing input = I_DC_LVL

Table 128. Register MISC_CTRL (address 0Bh) *…continued*
Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
3 to 2	Q_LEV_CTRL[1:0]	R/W		specifies output from CDI for Q path
			00	**normal operation (CDI data output sent to digital signal processing input)**
			01	id data enable = 1: the normal operation; if data enable = 0: digital signal processing input = Q_DC_LEVEL register value
			10	digital signal processing input = Q_DC_LEVEL
			11	digital signal processing input = Q_DC_LEVEL
1 to 0	CDI_MODE[1:0]	R/W		specifies CDI mode
			00	**cdi_mode 0 (^2 mode)**
			01	cdi_mode 1 (^4 mode)
			10	cdi_mode 2 (^8 mode)
			11	not used

Table 129. LDS/MDS of I/Q DC levels registers (address 0Ch to 0Fh) bit description
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0Ch	I_DC_LVL_LSB	7 to 0	I_DC_LEVEL[7:0]	R/W		I_DC_LEVEL
					-	least significant 8 bits for I_DC_LEVEL
0Dh	I_DC_LVL_MSB	7 to 0	I_DC_LEVEL[15:8]	R/W		I_DC_LEVEL
					-	most significant 8 bits for I_DC_LEVEL
0Eh	Q_DC_LVL_LSB	7 to 0	Q_DC_LEVEL[7:0]	R/W		Q_DC_LEVEL
					-	least significant 8 bits for Q_DC_LEVEL
0Fh	Q_DC_LVL_MSB	7 to 0	Q_DC_LEVEL[15:8]	R/W		Q_DC_LEVEL
					-	most significant 8 bits for Q_DC_LEVEL

Table 130. TYPE_ID registers (address 1Bh to 1Eh) bit description
Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
1Bh	TYPE_ID_0	7 to 0	TYPE_ID_0[7:0]	R	-	
1Ch	TYPE_ID_1	7 to 0	TYPE_ID_1[7:0]	R	-	
1Dh	TYPE_ID_2	7 to 0	TYPE_ID_2[7:0]	R	-	
1Eh	TYPE_ID_3	7 to 0	TYPE_ID_3[7:0]	R	-	

Table 131. Register PAGE_ADD (address 1Fh)
Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
4 to 0	PAGE[4:0]	R/W		Page address

10.17.8 Page x10/x11 : RX physical layer

This page specifies the configuration ot the physical layer of the deserializer. Page x10 controls the various features as the equalizer and the common-mode voltage or resistor termination. Page x11 monitors the status of the previous controls.

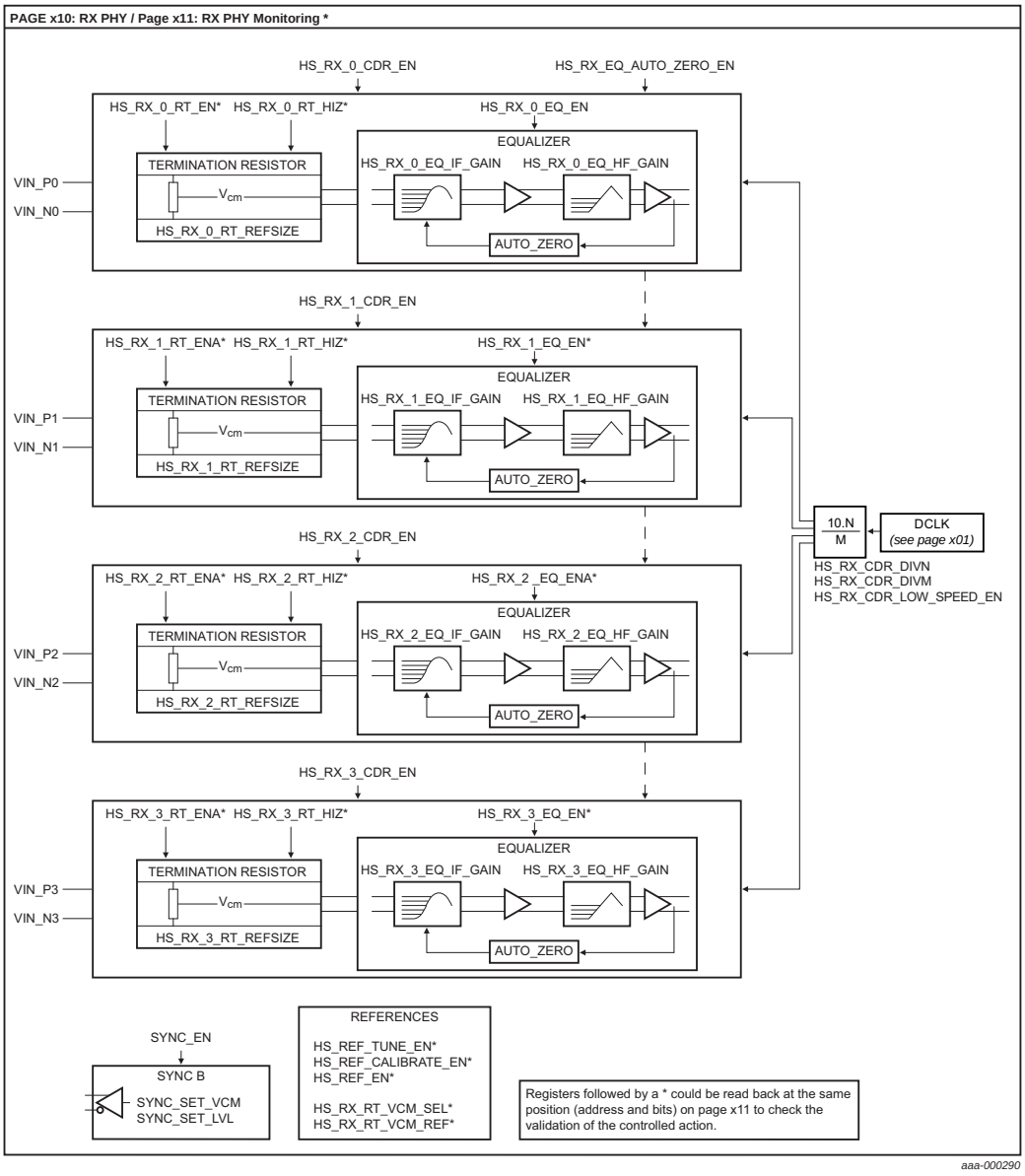


Fig 31. Page x10: RX PHY control

10.17.8.1 Page x10 register allocation map

Table 132 shows an overview of all registers on page x10.

Table 132. Page x10 register allocation map

Address		Register name	R/W	Bit definition								Default	
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
0	00h	HS_REF_EN	R/W	-	-	-	-	-	HS_REF_TUNE_EN	HS_REF_CAL_EN	HS_REF_EN	0000 0101	05h
1	01h	HS_REF_POLY_TRIM	R/W	-	-	HS_REF_POLY_TRIM[5:0]						0000 0000	00h
2	02h	HS_RX_CDR_DIV	R/W	HS_RX_CDR_LOW_SPEED_EN	HS_RX_CDR_DIVM[1:0]		HS_RX_CDR_DIVN[4:0]					0000 0010	02h
3	03h	HS_RX_CDR_CP	R/W	HS_RX_CDR_CP_IUP[3:0]				HS_RX_CDR_CP_IDW[3:0]				1111 1111	FFh
4	04h	HS_RX_CDR_LOOP	R/W	HS_RX_CDR_LOOP_RZ_TRACK[2:0]			HS_RX_CDR_LOOP_RZ_RUNIN[2:0]			HS_RX_CDR_LOOP_CAP[1:0]		0001 0111	17h
5	05h	HS_RX_CDR_EN_0	R/W	-	-	-	-	HS_RX_3_CDR_EN	HS_RX_2_CDR_EN	HS_RX_1_CDR_EN	HS_RX_0_CDR_EN	0000 1111	0Fh
6	06h	HS_RX_CDR_EN_1	R/W	HS_RX_3_CDR_FACQ_EN	HS_RX_2_CDR_FACQ_EN	HS_RX_1_CDR_FACQ_EN	HS_RX_0_CDR_FACQ_EN	HS_RX_3_CDR_TRACK_DATA_EN	HS_RX_2_CDR_TRACK_DATA_EN	HS_RX_1_CDR_TRACK_DATA_EN	HS_RX_0_CDR_TRACK_DATA_EN	0000 0000	00h
7	07h	HS_RX_EQ_CTRL	R/W	-	-	HS_RX_EQ_TEST_DUTY_EN	HS_RX_EQ_AUTO_ZERO_EN	HS_RX_3_EQ_EN	HS_RX_2_EQ_EN	HS_RX_1_EQ_EN	HS_RX_0_EQ_EN	0001 1111	1Fh
8	08h	HS_RX_0_EQ_GAIN	R/W	-	-	HS_RX_0_EQ_HF_GAIN[1:0]		-	HS_RX_0_EQ_IF_GAIN[2:0]			0000 0000	00h
9	09h	HS_RX_1_EQ_GAIN	R/W	-	-	HS_RX_1_EQ_HF_GAIN[1:0]		-	HS_RX_1_EQ_IF_GAIN[2:0]			0000 0000	00h
10	0Ah	HS_RX_2_EQ_GAIN	R/W	-	-	HS_RX_2_EQ_HF_GAIN[1:0]		-	HS_RX_2_EQ_IF_GAIN[2:0]			0000 0000	00h
11	0Bh	HS_RX_3_EQ_GAIN	R/W	-	-	HS_RX_3_EQ_HF_GAIN[1:0]		-	HS_RX_3_EQ_IF_GAIN[2:0]			0000 0000	00h
12	0Ch	HS_RX_0_EQ_OFFSET	R/W	-	HS_RX_0_EQ_INPUT_SHORT	HS_RX_0_EQ_OFFSET[5:0]						0000 0000	00h

Table 132. Page x10 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default	
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
13	0Dh	HS_RX_1_EQ_OFFSET	R/W	-	HS_RX_1_EQ_INPUT_SHORT	HS_RX_1_EQ_OFFSET[5:0]						0000 0000	00h
14	0Eh	HS_RX_2_EQ_OFFSET	R/W	-	HS_RX_2_EQ_INPUT_SHORT	HS_RX_2_EQ_OFFSET[5:0]						0000 0000	00h
15	0Fh	HS_RX_3_EQ_OFFSET	R/W	-	HS_RX_3_EQ_INPUT_SHORT	HS_RX_3_EQ_OFFSET[5:0]						0000 0000	00h
16	10h	HS_RX_RT_VCM	R/W	-	-	HS_RX_RT_VCM_SEL	HS_RX_RT_VCM_REF[4:0]					0010 0101	25h
17	11h	HS_RX_RT_CTRL	R/W	HS_RX_3_RT_HIZ_EN	HS_RX_2_RT_HIZ_EN	HS_RX_1_RT_HIZ_EN	HS_RX_0_RT_HIZ_EN	HS_RX_3_RT_EN	HS_RX_2_RT_EN	HS_RX_1_RT_EN	HS_RX_0_RT_EN	0000 1111	0Fh
18	12h	HS_RX_0_RT_REFSIZE	R/W	HS_RX_0_RT_REFSIZE[8:1]								0101 0000	50h
19	13h	HS_RX_1_RT_REFSIZE	R/W	HS_RX_1_RT_REFSIZE[8:1]								0101 0000	50h
20	14h	HS_RX_2_RT_REFSIZE	R/W	HS_RX_2_RT_REFSIZE[8:1]								0101 0000	50h
21	15h	HS_RX_3_RT_REFSIZE	R/W	HS_RX_3_RT_REFSIZE[8:1]								0101 0000	50h
22	16h	HS_RX_X_RT_REFSIZE	R/W	-	-	-	-	HS_RX_3_RT_REFSIZE[0]	HS_RX_2_RT_REFSIZE[0]	HS_RX_1_RT_REFSIZE[0]	HS_RX_0_RT_REFSIZE[0]	0000 0000	00h
29	1Dh	SYNC_CFG_CTRL	R/W	SYNC_EN	SYNC_SET_VCM[6:4]			SYNC_SET_LVL[3:0]				1000 0000	80h
31	1Fh	PAGE_ADDRESS	R/W	-	-	-	PAGE[4:0]					0000 0000	00h

10.17.8.2 Page x10 bit definition detailed description

The tables in this section contain detailed descriptions of the page x10 registers.

Table 133. HS_REF_EN register (address 00h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
2	HS_REF_TUNE_EN	R/W		continuous calibration mode
			0	hs_ref is not in continuous calibration mode
			1	hs_ref is in continuous calibration mode
1	HS_REF_CAL_EN	R/W		calibration mode
			0	hs_ref is not in calibration mode
			1	hs_ref in calibration mode (when hs_ref_tune_en is low)
0	HS_REF_EN	R/W		hs_ref module
			0	disabled (power-down)
			1	enabled (active)

Table 134. HS_REF_POLY_TRIM register (address 01h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
5 to 0	HS_REF_POLY_TRIM[5:0]	R/W	-	hs_ref poly trimming inputs (actually not used)

Table 135. HS_RX_CDR_DIV register (address 02h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7	HS_RX_CDR_LOW_SPEED_EN	R/W		low speed mode
			0	disabled
			1	enabled
6 to 5	HS_RX_CDR_DIVM[1:0]	R/W	-	divm ratio used to divide refclk (predivider)
4 to 0	HS_RX_CDR_DIVN[4:0]	R/W	-	divn ratio used in CDR reference loop

Table 136. HS_RX_CDR_CP register(address 03h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 4	HS_RX_CDR_CP_IUP[3:0]	R/W	-	sets charge pump up-current (~0.5 to ~ 8.0 μA)
3 to 0	HS_RX_CDR_CP_IDW[3:0]	R/W	-	sets charge pump down-current (~0.5 to ~8.0 μA)

Table 137. HS_RX_CDR_LOOP register(address 04h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	HS_RX_CDR_LOOP_RZ_TRACK[2:0]	R/W	-	CDR loop resistance value in track mode
4 to 2	HS_RX_CDR_LOOP_RZ_RUNIN[2:0]	R/W	-	CDR loop resistance value in run-in mode
1 to 0	HS_RX_CDR_LOOP_CAP[1:0]	R/W	-	CDR loop capacitance value

Table 138. HS_RX_CDR_EN registers (address 05h to 06h) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
05h	HS_RX_CDR_EN_0	3	HS_RX_3_CDR_EN	R/W	0	CDR of rx of lane 3 disabled (power-down)
					1	CDR of rx of lane 3 enabled (active)
		2	HS_RX_2_CDR_EN	R/W	0	CDR of rx_ln2 disabled (power-down)
					1	CDR of rx_ln2 enabled (active)
		1	HS_RX_1_CDR_EN	R/W	0	CDR of rx_ln1 disabled (power-down)
					1	CDR of rx_ln1 enabled (active)
		0	HS_RX_0_CDR_EN	R/W	0	CDR of rx_ln0 disabled (power-down)
					1	CDR of rx_ln0 enabled (active)
06h	HS_RX_CDR_EN_1	7	HS_RX_3_CDR_FACQ_EN	R/W		frequency acquisition mode
					0	CDR_ln3 frequency acquisition mode disabled
					1	CDR_ln3 frequency acquisition mode enabled
		6	HS_RX_2_CDR_FACQ_EN	R/W	0	CDR_ln2 frequency acquisition mode disabled
					1	CDR_ln2 frequency acquisition mode enabled
		5	HS_RX_1_CDR_FACQ_EN	R/W	0	CDR_ln1 frequency acquisition mode disabled
					1	CDR_ln1 frequency acquisition mode enabled
		4	HS_RX_0_CDR_FACQ_EN	R/W	0	CDR_ln0 frequency acquisition mode disabled
					1	CDR_ln0 frequency acquisition mode enabled
		3	HS_RX_3_CDR_TRACK_DATA_EN	R/W		data tracking mode
					0	CDR_ln3 in pfd mode (reference loop)
					1	CDR_ln3 in data tracking mode (normal mode)
		2	HS_RX_2_CDR_TRACK_DATA_EN	R/W	0	CDR_ln2 in pfd mode (reference loop)
					1	CDR_ln2 in data tracking mode (normal mode)

Table 138. HS_RX_CDR_EN registers (address 05h to 06h) bit description *…continued*

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
		1	HS_RX_1_CDR_TRACK_DATA_EN	R/W	0	CDR_ln1 in pfd mode (reference loop)
					1	CDR_ln1 in data tracking mode (normal mode)
		0	HS_RX_0_CDR_TRACK_DATA_EN	R/W	0	CDR_ln0 in pfd mode (reference loop)
					1	CDR_ln0 in data tracking mode (normal mode)

Table 139. HS_RX_EQ_CTRL register (address 07h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
5	HS_RX_EQ_TST_DTY_EN	R/W		Equalizer duty cycle test
			0	disabled (for all lanes)
			1	enabled (for all lanes)
4	HS_RX_EQ_AUTO_ZERO_EN	R/W		Equalizer auto zero mode
			0	disabled (for all lanes)
			1	enabled (for all lanes)
3	HS_RX_3_EQ_EN	R/W		Equalizer of rx_ln3
			0	disabled (power-down)
			1	enabled (active)
2	HS_RX_2_EQ_EN	R/W		Equalizer of rx_ln2
			0	disabled (power-down)
			1	enabled (active)
1	HS_RX_1_EQ_EN	R/W		Equalizer of rx_ln1
			0	disabled (power-down)
			1	enabled (active)
0	HS_RX_0_EQ_EN	R/W		Equalizer of rx_ln0
			0	disabled (power-down)
			1	enabled (active)

Table 140. Equalizer gain registers (address 08h to 0Bh) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
08h	HS_RX_0_EQ_GAIN	5 to 4	HS_RX_0_EQ_HF_GAIN[1:0]	R/W	-	sets hf-gain for rx_ln0 equalizer
		2 to 0	HS_RX_0_EQ_IF_GAIN[2:0]		-	sets if-gain for rx_ln0 equalizer
09h	HS_RX_1_EQ_GAIN	5 to 4	HS_RX_1_EQ_HF_GAIN[1:0]	R/W	-	sets hf-gain for rx_ln1 equalizer
		2 to 0	HS_RX_1_EQ_IF_GAIN[2:0]		-	sets if-gain for rx_ln1 equalizer

Table 140. Equalizer gain registers (address 08h to 0Bh) bit description *...continued*

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0Ah	HS_RX_2_EQ_GAIN	5 to 4	HS_RX_2_EQ_HF_GAIN[1:0]	R/W	-	sets hf-gain for rx_ln2 equalizer
		2 to 0	HS_RX_2_EQ_IF_GAIN[2:0]		-	sets if-gain for rx_ln2 equalizer
0Bh	HS_RX_3_EQ_GAIN	5 to 4	HS_RX_3_EQ_HF_GAIN[1:0]	R/W	-	sets hf-gain for rx_ln3 equalizer
		2 to 0	HS_RX_3_EQ_IF_GAIN[2:0]		-	sets if-gain for rx_ln3 equalizer

Table 141. Equalizer offset registers (address 0Ch to 0Fh) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0Ch	HS_RX_0_EQ_OFS	6	HS_RX_0_EQ_INPUT_SHORT	R/W		rx_ln0 input equalizer shorted to V_{DD}
					0	no action
					1	rx_ln0 equalizer input shorted to V_{DD}
		5 to 0	HS_RX_0_EQ_OFFSET[5:0]	R/W	-	rx_ln0 equalizer offset adjustment input
0Dh	HS_RX_1_EQ_OFS	6	HS_RX_1_EQ_INPUT_SHORT	R/W		rx_ln1 input equalizer shorted to V_{DD}
					0	no action
					1	rx_ln1 equalizer input shorted to V_{DD}
		5 to 0	HS_RX_1_EQ_OFFSET[5:0]	R/W	-	rx_ln1 equalizer offset adjustment input
0Eh	HS_RX_2_EQ_OFS	6	HS_RX_2_EQ_INPUT_SHORT	R/W		rx_ln2 input equalizer shorted to V_{DD}
					0	no action
					1	rx_ln2 equalizer input shorted to V_{DD}
		5 to 0	HS_RX_2_EQ_OFFSET[5:0]	R/W	-	rx_ln2 equalizer offset adjustment input
0Fh	HS_RX_3_EQ_OFS	6	HS_RX_3_EQ_INPUT_SHORT	R/W	-	rx_ln3 input equalizer shorted to V_{DD}
					0	no action
					1	rx_ln3 equalizer input shorted to V_{DD}
		5 to 0	HS_RX_3_EQ_OFFSET[5:0]	R/W	-	rx_ln3 equalizer offset adjustment input

Table 142. HS_RX_RT_VCM register (address 10h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
5	HS_RX_RT_VCM_SEL	R/W		rx_rt modules configuration
			0	do not use
			1	rx_rt_modules configured for RX-use (all lanes)
4 to 0	HS_RX_RT_VCM_REF[4:0]	R/W	-	sets common-mode reference for hs_rx_rt (all lanes)

Table 143. HS_RX_RT_CTRL register (address 11h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7	HS_RX_3_RT_HIZ_EN	R/W		hs_rx_ln3 input
			0	100 Ω (differential impedance)
			1	high ohmic
6	HS_RX_2_RT_HIZ_EN	R/W		hs_rx_ln2 input
			0	100 Ω (differential impedance)
			1	high ohmic
5	HS_RX_1_RT_HIZ_EN	R/W		hs_rx_ln1 input
			0	100 Ω (differential impedance)
			1	high ohmic
4	HS_RX_0_RT_HIZ_EN	R/W		hs_rx_ln0 input
			0	100 Ω (differential impedance)
			1	high ohmic
3	HS_RX_3_RT_EN	R/W		Termination of rx_ln3
			0	disabled (power-down)
			1	enabled (active)
2	HS_RX_2_RT_EN	R/W		Termination of rx_ln2
			0	disabled (power-down)
			1	enabled (active)
1	HS_RX_1_RT_EN	R/W		Termination of rx_ln1
			0	disabled (power-down)
			1	enabled (active)
0	HS_RX_1_RT_EN	R/W		Termination of rx_ln0
			0	disabled (power-down)
			1	enabled (active)

Table 144. Termination impedance fine-tuning (MSBs) registers (address 12h to 15h) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
12h	HS_RX_0_RT_REFSIZE	7 to 0	HS_RX_0_RT_REF_SIZE[8:1]	R/W	-	most significant 8 bits of termination impedance fine-tuning lane 0
13h	HS_RX_1_RT_REFSIZE	7 to 0	HS_RX_1_RT_REF_SIZE[8:1]	R/W	-	most significant 8 bits of termination impedance fine-tuning lane 1
14h	HS_RX_2_RT_REFSIZE	7 to 0	HS_RX_2_RT_REF_SIZE[8:1]	R/W	-	most significant 8 bits of termination impedance fine-tuning lane 2
15h	HS_RX_3_RT_REFSIZE	7 to 0	HS_RX_3_RT_REF_SIZE[8:1]	R/W	-	most significant 8 bits of termination impedance fine-tuning lane 3

Table 145. HS_RX_X_RT_REFSIZE register (address 16h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
3	HS_RX_3_RT_REFSIZE	R/W	-	least significant bit of termination impedance fine-tuning lane 3
2	HS_RX_2_RT_REFSIZE	R/W	-	least significant bit of termination impedance finetuning lane 2
1	HS_RX_1_RT_REFSIZE	R/W	-	least significant bit of termination impedance fine-tuning lane 1
0	HS_RX_1_RT_REFSIZE	R/W	-	least significant bit of termination impedance fine-tuning lane 0

Table 146. SYNC_CFG_CTRL register (address 1Dh) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7	SYNC_EN	R/W		synchronization buffer
			0	disabled (power-down)
			1	enabled (active)
6 to 4	SYNC_SET_VCM[6:4]	R/W	-	sets common-mode output voltage of synchronization buffer
3 to 0	SYNC_SET_LVL[3:0]	R/W	-	sets output levels (swing) of synchronization buffer

Table 147. PAGE_ADDRESS register (address 1Fh) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
4 to 0	PAGE[4:0]	R/W	-	page address

10.17.8.3 Page x11 register allocation map

Table 148 shows an overview of all registers on page x11.

Table 148. Page 11 register allocation map

Address		Register name	R/W	Bit definition								Default	
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
0	00h	I_HS_REF_EN	R	-	-	-	-	-	I_HS_REF_TUNE_EN	I_HS_REF_CALIBRATE_EN	I_HS_REF_EN	0000 0101	05h
1	01h	I_HS_REF_POLY_TRIM	R	-	-	I_HS_REF_POLY_TRIM[5:0]						0000 0000	00h
4	04h	I_HS_RX_CDR_LOOP	R	I_HS_RX_CDR_LOOP_RZ[2:0]			-	-	-	-	-	0001 0111	17h
5	05h	I_HS_RX_CDR_ENA_0	R	-	-	-	-	I_HS_RX3_CDR_EN	I_HS_RX2_CDR_EN	I_HS_RX1_CDR_EN	I_HS_RX0_CDR_EN	0000 1111	0Fh
6	06h	I_HS_RX_CDR_ENA_1	R	-	-	-	-	I_HS_RX3_CDR_TRACK_DATA_EN	I_HS_RX2_CDR_TRACK_DATA_EN	I_HS_RX1_CDR_TRACK_DATA_EN	I_HS_RX0_CDR_TRACK_DATA_EN	0000 0000	00h
7	07h	I_HS_RX_EQ_CNTRL	R	-	-	I_HS_RX_EQ_TEST_DUTY_EN	I_HS_RX_EQ_AUTO_ZERO_EN	I_HS_RX3_EQ_EN	I_HS_RX2_EQ_EN	I_HS_RX1_EQ_EN	I_HS_RX0_EQ_EN	0001 1111	1Fh
12	0Ch	I_HS_RX_0_EQ_OFS	R	-	I_HS_RX0_EQ_INPUT_SHORT	I_HS_RX0_EQ_OFFSET[5:0]						0000 0000	00h
13	0Dh	I_HS_RX_1_EQ_OFS	R	-	I_HS_RX1_EQ_INPUT_SHORT	I_HS_RX1_EQ_OFFSET[5:0]						0000 000	00h
14	0Eh	I_HS_RX_2_EQ_OFS	R	-	I_HS_RX2_EQ_INPUT_SHORT	I_HS_RX2_EQ_OFFSET[5:0]						0000 0000	00h
15	0Fh	I_HS_RX_3_EQ_OFS	R	-	I_HS_RX3_EQ_INPUT_SHORT	I_HS_RX3_EQ_OFFSET[5:0]						0000 0000	00h
17	11h	I_HS_RX_RT_CNTRL	R	-	-	-	-	I_HS_RX_3_RT_EN	I_HS_RX_2_RT_EN	I_HS_RX_1_RT_EN	I_HS_RX_0_RT_EN		
25	19h	HS_RX_0_MON	R	-	-	-	-	HS_RX_0_EQ_TEST_DUTY_OUT	HS_RX_0_EQ_OFS_POL	HS_RX_0_LOCK_REFCLOCK	HS_RX_0_CDR_FACQ_BUSY		

Table 148. Page 11 register allocation map *…continued*

Address		Register name	R/W	Bit definition								Default	
				Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bin	Hex
26	1Ah	HS_RX_1_MON	R	-	-	-	-	HS_RX_1_EQ_TEST_DUTY_OUT	HS_RX_1_EQ_OFS_POL	HS_RX_1_LOCK_REFCLOCK	HS_RX_1_CDR_FACQ_BUSY		
27	1Bh	HS_RX_2_MON	R	-	-	-	-	HS_RX_2_EQ_TEST_DUTY_OUT	HS_RX_2_EQ_OFS_POL	HS_RX_2_LOCK_REFCLOCK	HS_RX_2_CDR_FACQ_BUSY		
28	1Ch	HS_RX_3_MON	R	-	-	-	-	HS_RX_3_EQ_TEST_DUTY_OUT	HS_RX_3_EQ_OFS_POL	HS_RX_3_LOCK_REFCLOCK	HS_RX_3_CDR_FACQ_BUSY		
29	1Dh	HS_RX_IFIX_MON	R	-	-	-	-	-	-	-	HS_REF_IFIX_LOW		
30	1Eh	HS_RX_VERSION	R	RX_PHY_VERSION_NO[7:0]								0000 0001	01h
31	1Fh	PAGE_ADDRESS	R/W	-	-	-	PAGE[4:0]					0000 0000	00h

10.17.8.4 Page x11 bit definition detailed description

Table 149. I_HS_REF_EN register (address 00h) bit description
Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
2	HS_REF_TUNE_EN	R		continuous calibration mode
			0	hs_ref is not in continuous calibration mode
			1	hs_ref is in continuous calibration mode
1	HS_REF_CAL_EN	R		calibration mode
			0	hs_ref is not in calibration mode
			1	hs_ref in calibration mode (when hs_ref_tune_en is low)
0	HS_REF_EN	R		hs_ref module
			0	disabled (power-down)
			1	enabled (active)

Table 150. I_HS_REF_POLY_TRIM register (address 01h) bit description
Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
5 to 0	HS_REF_POLY_TRIM[5:0]	R	-	hs_ref poly trimming inputs (actually not used)

Table 151. I_HS_RX_CDR_LOOP register(address 04h) bit description
Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 5	HS_RX_CDR_LOOP_RZ[2:0]	R	-	actual CDR loop resistance value

Table 152. I_HS_RX_CDR_EN registers (address 05h to 06h) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
05h	HS_RX_CDR_EN_0	3	HS_RX_3_CDR_EN	R	0	CDR of rx_ln3 disabled (power-down)
					1	CDR of rx_ln3 enabled (active)
		2	HS_RX_2_CDR_EN	R	0	CDR of rx_ln2 disabled (power-down)
					1	CDR of rx_ln2 enabled (active)
		1	HS_RX_1_CDR_EN	R	0	CDR of rx_ln1 disabled (power-down)
					1	CDR of rx_ln1 enabled (active)
		0	HS_RX_0_CDR_EN	R	0	CDR of rx_ln0 disabled (power-down)
					1	CDR of rx_ln0 enabled (active)
06h	I_HS_RX_CDR_EN_1	3	HS_RX_3_CDR_TRACK_DATA_EN	R		data tracking mode
					0	CDR_ln3 in pfd mode (reference loop)
					1	CDR_ln3 in data tracking mode (normal mode)
		2	HS_RX_2_CDR_TRACK_DATA_EN	R	0	CDR_ln2 in pfd mode (reference loop)
					1	CDR_ln2 in data tracking mode (normal mode)
		1	HS_RX_1_CDR_TRACK_DATA_EN	R	0	CDR_ln1 in pfd mode (reference loop)
					1	CDR_ln1 in data tracking mode (normal mode)
		0	HS_RX_0_CDR_TRACK_DATA_EN	R	0	CDR_ln0 in pfd mode (reference loop)
					1	CDR_ln0 in data tracking mode (normal mode)

Table 153. I_HS_RX_EQ_CTRL register (address 07h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
5	HS_RX_EQ_TST_DTY_EN	R		Equalizer duty cycle test
			0	disabled (for all lanes)
			1	enabled (for all lanes)
4	HS_RX_EQ_AUTO_ZERO_EN	R		Equalizer auto zero mode
			0	disabled (for all lanes)
			1	enabled (for all lanes)
3	HS_RX_3_EQ_EN	R		Equalizer of rx_ln3
			0	disabled (power-down)
			1	enabled (active)

Table 153. I_HS_RX_EQ_CTRL register (address 07h) bit description *...continued*

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
2	HS_RX_2_EQ_EN	R		Equalizer of rx_ln2
			0	disabled (power-down)
			1	enabled (active)
1	HS_RX_1_EQ_EN	R		Equalizer of rx_ln1
			0	disabled (power-down)
			1	enabled (active)
0	HS_RX_0_EQ_EN	R		Equalizer of rx_ln0
			0	disabled (power-down)
			1	enabled (active)

Table 154. Equalizer offset registers (address 0Ch to 0Fh) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
0Ch	HS_RX_0_EQ_OFS	6	HS_RX_0_EQ_INPUT_SHORT	R		rx_ln0 input equalizer shorted to V_{DD}
					0	no action
					1	rx_ln0 equalizer input shorted to V_{DD}
		5 to 0	HS_RX_0_EQ_OFFSET[5:0]	R	-	rx_ln0 equalizer offset adjustment input
0Dh	HS_RX_1_EQ_OFS	6	HS_RX_1_EQ_INPUT_SHORT	R		rx_ln1 input equalizer shorted to V_{DD}
					0	no action
					1	rx_ln1 equalizer input shorted to V_{DD}
		5 to 0	HS_RX_1_EQ_OFFSET[5:0]	R	-	rx_ln1 equalizer offset adjustment input
0Eh	HS_RX_2_EQ_OFS	6	HS_RX_2_EQ_INPUT_SHORT	R		rx_ln2 input equalizer shorted to V_{DD}
					0	no action
					1	rx_ln2 equalizer input shorted to V_{DD}
		5 to 0	HS_RX_2_EQ_OFFSET[5:0]	R	-	rx_ln2 equalizer offset adjustment input
0Fh	HS_RX_3_EQ_OFS	6	HS_RX_3_EQ_INPUT_SHORT	R	-	rx_ln3 input equalizer shorted to V_{DD}
					0	no action
					1	rx_ln3 equalizer input shorted to V_{DD}
		5 to 0	HS_RX_3_EQ_OFFSET[5:0]	R	-	rx_ln3 equalizer offset adjustment input

Table 155. HS_RX_RT_CTRL register (address 11h) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7	HS_RX_3_RT_HIZ_EN	R		hs_rx_ln3 input
			0	100 Ω (differential impedance)
			1	high ohmic
6	HS_RX_2_RT_HIZ_EN	R		hs_rx_ln2 input
			0	100 Ω (differential impedance)
			1	high ohmic
5	HS_RX_1_RT_HIZ_EN	R		hs_rx_ln1 input
			0	100 Ω (differential impedance)
			1	high ohmic
4	HS_RX_0_RT_HIZ_EN	R		hs_rx_ln0 input
			0	100 Ω (differential impedance)
			1	high ohmic
3	HS_RX_3_RT_EN	R		Termination of rx_ln3
			0	disabled (power-down)
			1	enabled (active)
2	HS_RX_2_RT_EN	R		Termination of rx_ln2
			0	disabled (power-down)
			1	enabled (active)
1	HS_RX_1_RT_EN	R		Termination of rx_ln1
			0	disabled (power-down)
			1	enabled (active)
0	HS_RX_1_RT_EN	R		Termination of rx_ln0
			0	disabled (power-down)
			1	enabled (active)

Table 156. HS_RX monitor registers (address 19h to 1Ch) bit description

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
19h	HS_RX_0_MON	3	HS_RX_0_EQ_TST_DTY_OUT	R		actual state hs_rx_0_eq_test_duty_out
		2	HS_RX_0_EQ_OFS_POL	R		hs_rx_ln0 equalizer offset
					0	negative
					1	positive
		1	HS_RX_0_LOCK_REF_CLK	R		hs_rx_0 lock to reference clock
					0	not locked to reference clock (pfd mode)
					1	locked to reference clock (pfd mode)
		0	HS_RX_0_CDR_FACQ_BUSY	R	-	actual state hs_rx_0_eq_test_duty_out (not used)

Table 156. HS_RX monitor registers (address 19h to 1Ch) bit description *...continued*

Default values are shown highlighted.

Address	Register	Bit	Symbol	Access	Value	Description
1Ah	HS_RX_1_MON	3	HS_RX_1_EQ_TST_DTY_OUT	R		actual state hs_rx_1_eq_test_duty_out
		2	HS_RX_1_EQ_OFS_POL	R		hs_rx_ln1 equalizer offset
					0	negative
					1	positive
		1	HS_RX_1_LOCK_REF_CLK	R		hs_rx_1 lock to reference clock
					0	not locked to reference clock (pfd mode)
					1	locked to reference clock (pfd mode)
		0	HS_RX_1_CDR_FACQ_BUSY	R	-	actual state hs_rx_1_eq_test_duty_out (not used)
1Bh	HS_RX_2_MON	3	HS_RX_2_EQ_TST_DTY_OUT	R		actual state hs_rx_2_eq_test_duty_out
		2	HS_RX_1_EQ_OFS_POL	R		hs_rx_ln2 equalizer offset
					0	negative
					1	positive
		1	HS_RX_2_LOCK_REF_CLK	R		hs_rx_2 lock to reference clock
					0	not locked to reference clock (pfd mode)
					1	locked to reference clock (pfd mode)
		0	HS_RX_2_CDR_FACQ_BUSY	R	-	actual state hs_rx_2_eq_test_duty_out (not used)
1Ch	HS_RX_3_MON	3	HS_RX_3_EQ_TST_DTY_OUT	R		actual state hs_rx_3_eq_test_duty_out
		2	HS_RX_3_EQ_OFS_POL	R		hs_rx_ln3 equalizer offset
					0	negative
					1	positive
		1	HS_RX_3_LOCK_REF_CLK	R		hs_rx_3 lock to reference clock
					0	not locked to reference clock (pfd mode)
					1	locked to reference clock (pfd mode)
		0	HS_RX_3_CDR_FACQ_BUSY	R	-	actual state hs_rx_3_eq_test_duty_out (not used)

Table 157. HS_RX_IFIX_MON register (address 1Dh) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
0	HS_REF_IFIX_LOW	R		status generated hs_ref (only meaningful when hs_ref_tune_en is low)
			0	generated hs_ref current is too low
			1	generated hs_ref current is too high

Table 158. HS_RX_VERSION register (address 1Eh) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
7 to 0	RX_PHY_VERSION_NO[7:0]	R/W	-	rx-phy version number

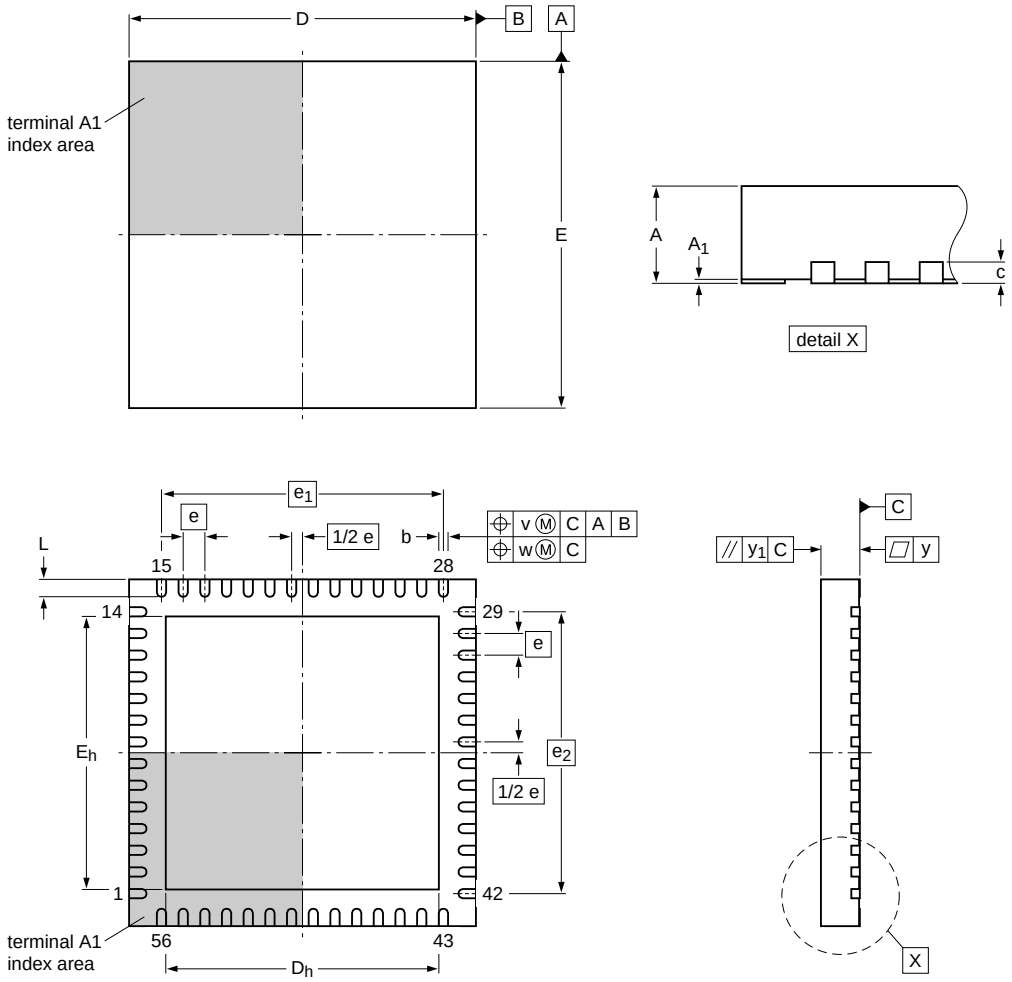
Table 159. PAGE_ADDRESS register (address 1Fh) bit description

Default values are shown highlighted.

Bit	Symbol	Access	Value	Description
4 to 0	PAGE[4:0]	R/W	-	page address

11. Package outline

HVQFN56: plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 x 8 x 0.85 mm **SOT684-8**



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.30		8.1	6.45	8.1	6.45				0.5				
mm	nom	0.85	0.02	0.21	0.2	8.0	6.30	8.0	6.30	0.5	6.5	6.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		7.9	6.15	7.9	6.15				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot684-8_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT684-8	- - -	- - -	- - -			~~09-01-07~~ 09-02-24

Fig 32. Package outline SOT684-8 (HVQFN56)

12. Abbreviations

Table 160. Abbreviations

Acronym	Description
B	BandWidth
BWA	Broadband Wireless Access
CDI	Clock Domain Interface
CDMA	Code Division Multiple Access
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
EDGE	Enhanced Data rates for GSM Evolution
FIR	Finite Impulse Response
GSM	Global System for Mobile communications
IF	Intermediate Frequency
IMD3	Third Order InterModulation
LMDS	Local Multipoint Distribution Service
LO	Local Oscillator
LVDS	Low-Voltage Differential Signaling
NCO	Numerically Controlled Oscillator
NMOS	Negative Metal-Oxide Semiconductor
PLL	Phase-Locked Loop
SFDR	Spurious-Free Dynamic Range
SPI	Serial Peripheral Interface
WCDMA	Wide band Code Division Multiple Access
WLL	Wireless Local Loop

13. Glossary

13.1 Static parameters

INL — The deviation of the transfer function from a best fit straight line (linear regression computation).

DNL — The difference between the ideal and the measured output value between successive DAC codes.

13.2 Dynamic parameters

Spurious-Free Dynamic Range (SFDR) — The ratio between the RMS value of the reconstructed output sine wave and the RMS value of the largest spurious observed (harmonic and non-harmonic, excluding DC component) in the frequency domain.

InterModulation Distortion (IMD) — From a dual-tone digital input sine wave (these two frequencies being close together), the intermodulation distortion products IMD2 and IMD3 (second order and third order components) are defined below.

IMD2 — The ratio between the RMS value of either tone and the RMS value of the worst second order intermodulation product.

IMD3 — The ratio between the RMS value of either tone and the RMS value of the worst third order intermodulation product.

Total Harmonic Distortion (THD) — The ratio between the RMS value of the harmonics of the output frequency and the RMS value of the output sine wave. Usually, the calculation of THD is done on the first 5 harmonics.

Signal-to-Noise Ratio (SNR) — The ratio between the RMS value of the reconstructed output sine wave and the RMS value of the noise excluding the harmonics and the DC component.

Restricted BandWidth Spurious-Free Dynamic Range ($SFDR_{RBW}$) — the ratio between the RMS value of the reconstructed output sine wave and the RMS value of the noise, including the harmonics, in a given bandwidth centered around f_{offset}.

14. Revision history

Table 161. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
DAC1628D1G25 v.1.1	20111010	Objective data sheet	-	DAC1628D1G25 v.1
Modifications:	• Section 1 “General description” has been updated. • Section 2 “Features and benefits” has been updated. • Section 3 “Applications” has been updated. • Table 5 “Characteristics” has been updated.			
DAC1628D1G25 v.1	20110907	Objective data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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